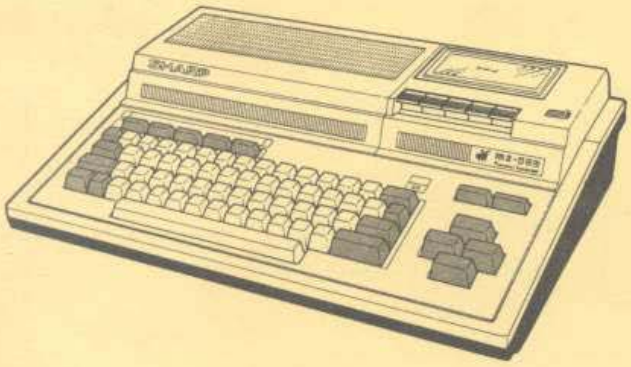
SHARP SERVICE MANUAL

CODE: 00ZMZ800////E



PERSONAL COMPUTER

MODEL MZ-800
MZ-1P16
MZ-1E20

Table of contents

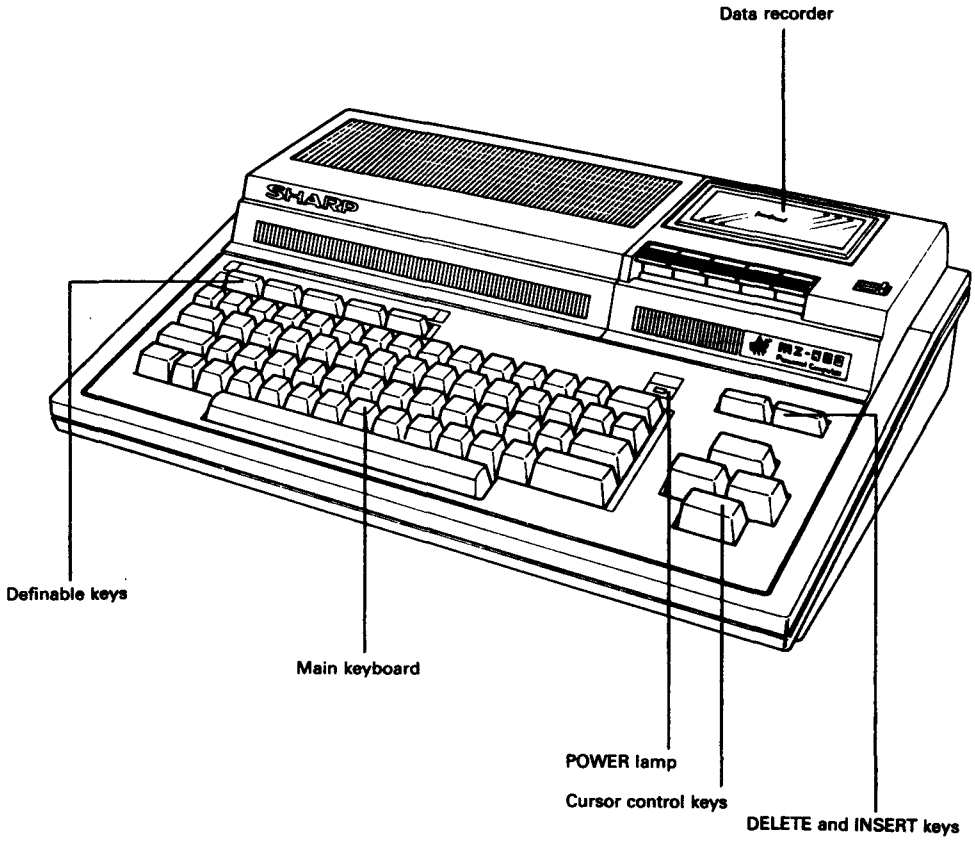
SHARP CORPORATION

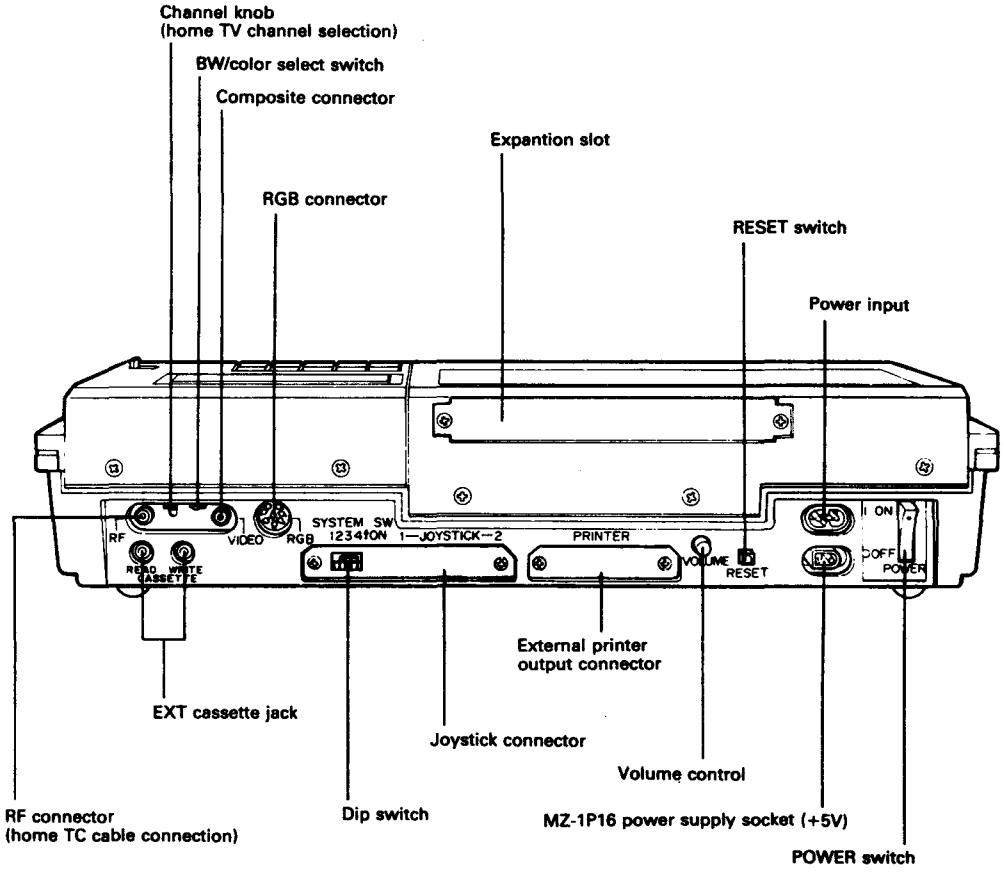
1. Specification

Item		Std/ Opt			
CPU			Z-80A		
Clock				3.5469 MHz	
MEMORY	ROM		MONITOR /CG	16 KB	MZ-700 – 4 KB MZ-800 – 8 KB CG – 4 KB
	RAM		SYSTEM	64 KB	
			VRAM	16 KB	
		OP	VRAM	16 KB	MZ-1R25
DISPLAY	I/F		Color	RF, VIDEO, RGB	16 colors handling internal encoder
	Display method			Bit map method PCG method	MZ-700 mode only
	Screen structure		Resolution	Frames	Display color
			320 × 200	1	4 colors
			640 × 200	1	1 color
		OP	320 × 200	1 or (2)	16 or (4) colors
		OP	640 × 200	1 or (2)	4 or (1) colors
	Color assignment			Choice out of 16 colors	
	Screen and character structures		Screen	80/40 characters	Software generated font
			Character	8 × 8	
	Screen control		Scroll	Character-scroll	
			Pallet	4 colors chosen out of 16 colors	
			Border color	Choice of 16 colors	
Internal I/O interface	Sound generation		6-octave, 3-chord	Internal speaker	SN76489 compatible
	Centronics interface		(Interface)	1 CH	Can be switched to MZ interface
	Plot printer	OP		MZ interface	
	Video output		RF, VIDEO (Analog RGB with the MZ-820F)		Color encoder (PAL) The I terminal to add for the RGB terminal
	Joystick		(Interface)	2 CH	ATARI compatible (joystick dedicated)
	Cassette tape recorder		(Interface)	READ/WRITE	
	Expansion slot			1 card	MZ-80B compatible
External I/O	MFD	OP		Two-sided, double density	MZ-1F02, MZ-1E05
	RS-232C	OP			MZ-8BiO3
	Joystick	OP			ATARI compatible
	MZ-DISK	OP			MZ-1E19, MZ-1F11
CRT	Color	OP	RGBI	16-color CRT	MZ-1D19 compatible
	B/W	OP	Video		MZ-1D04 compatible
Printer	80-column	OP		Dot matrix printer	MZ-80P5R
	80-column	OP		Plot printer	MZ-1P16
External control switch	Mode select		MZ-700 or MZ-800		Status $CE(D1)
	Printer interface specification		MZ or Centronics		

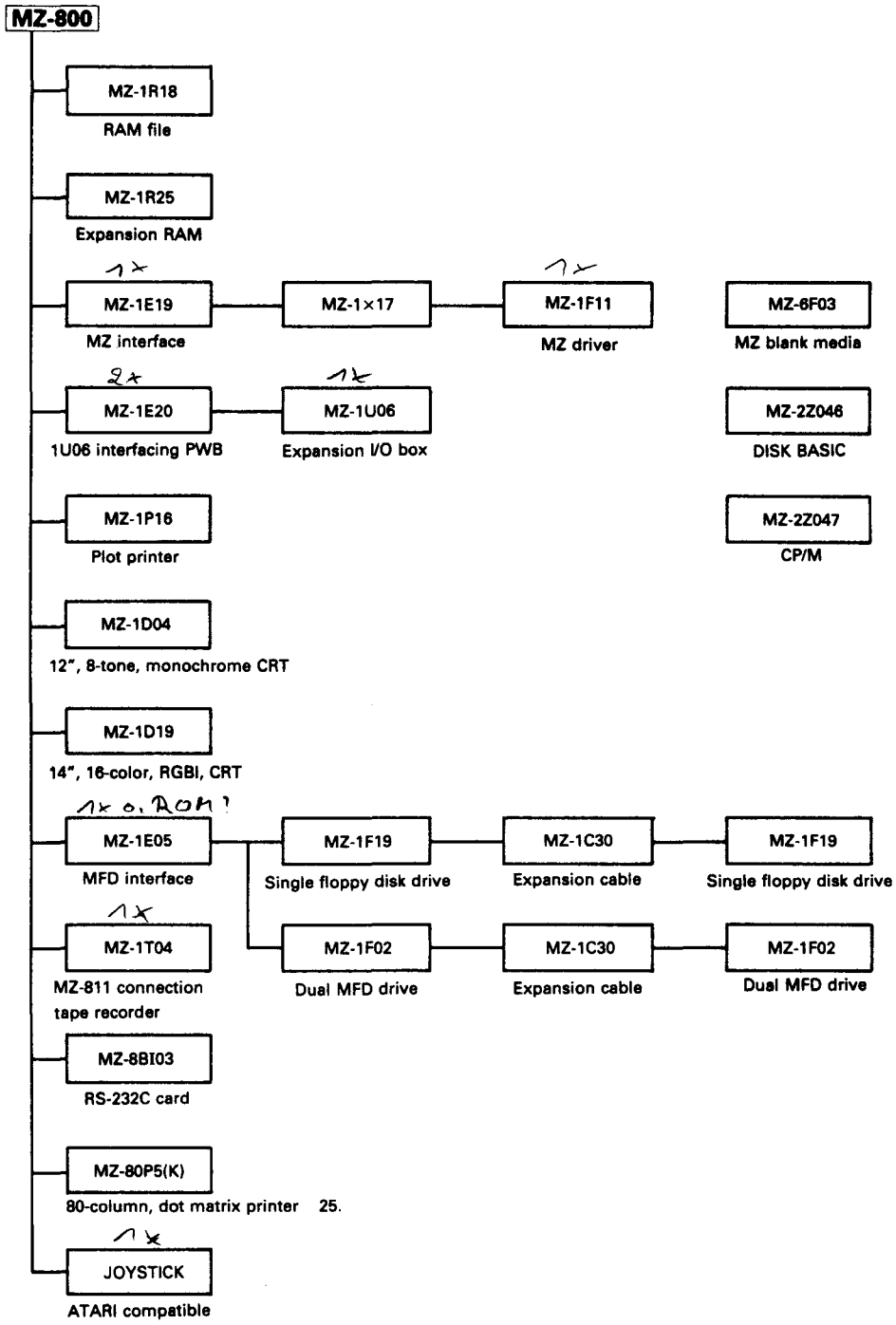
2. Parts identification

Front view

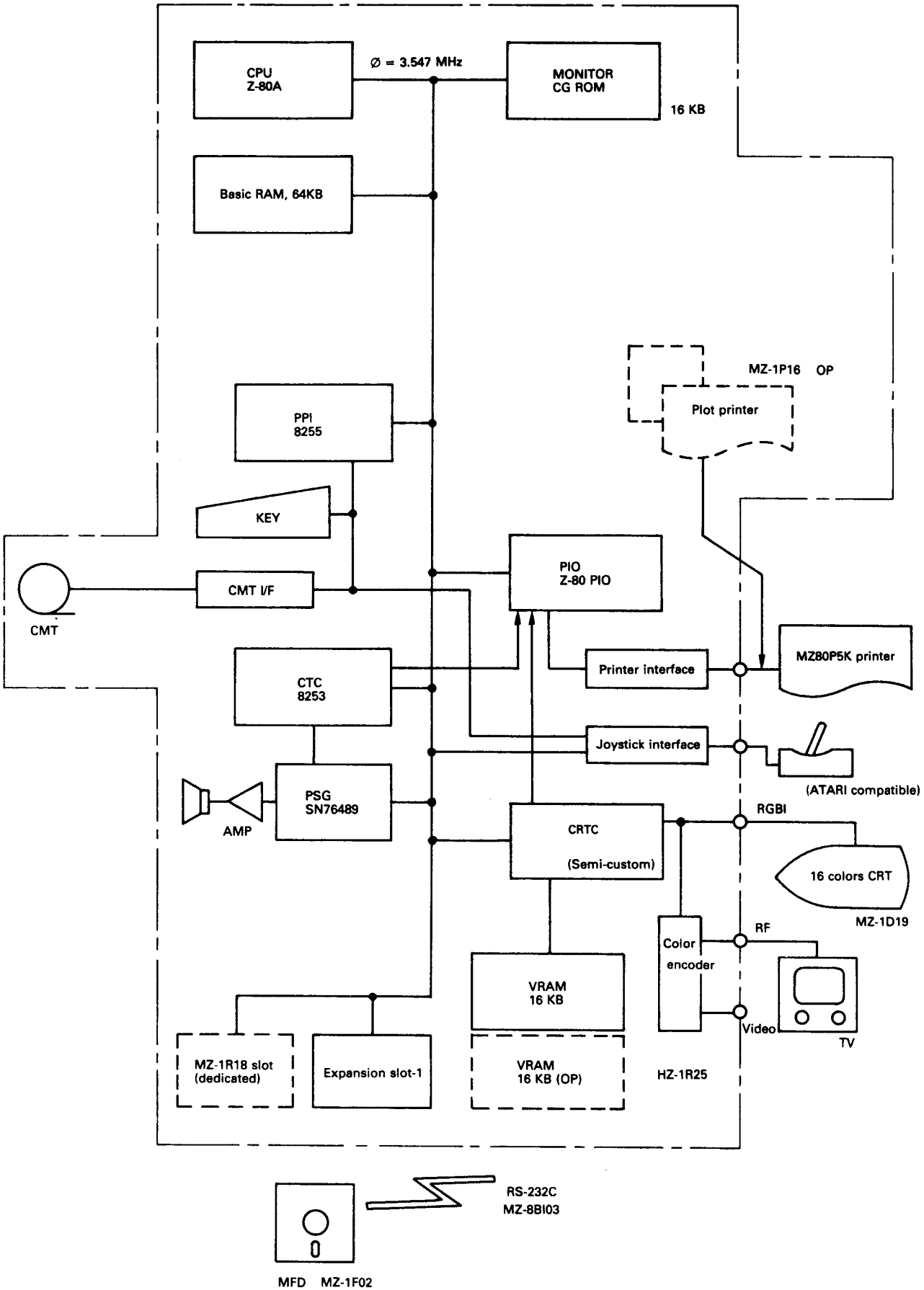




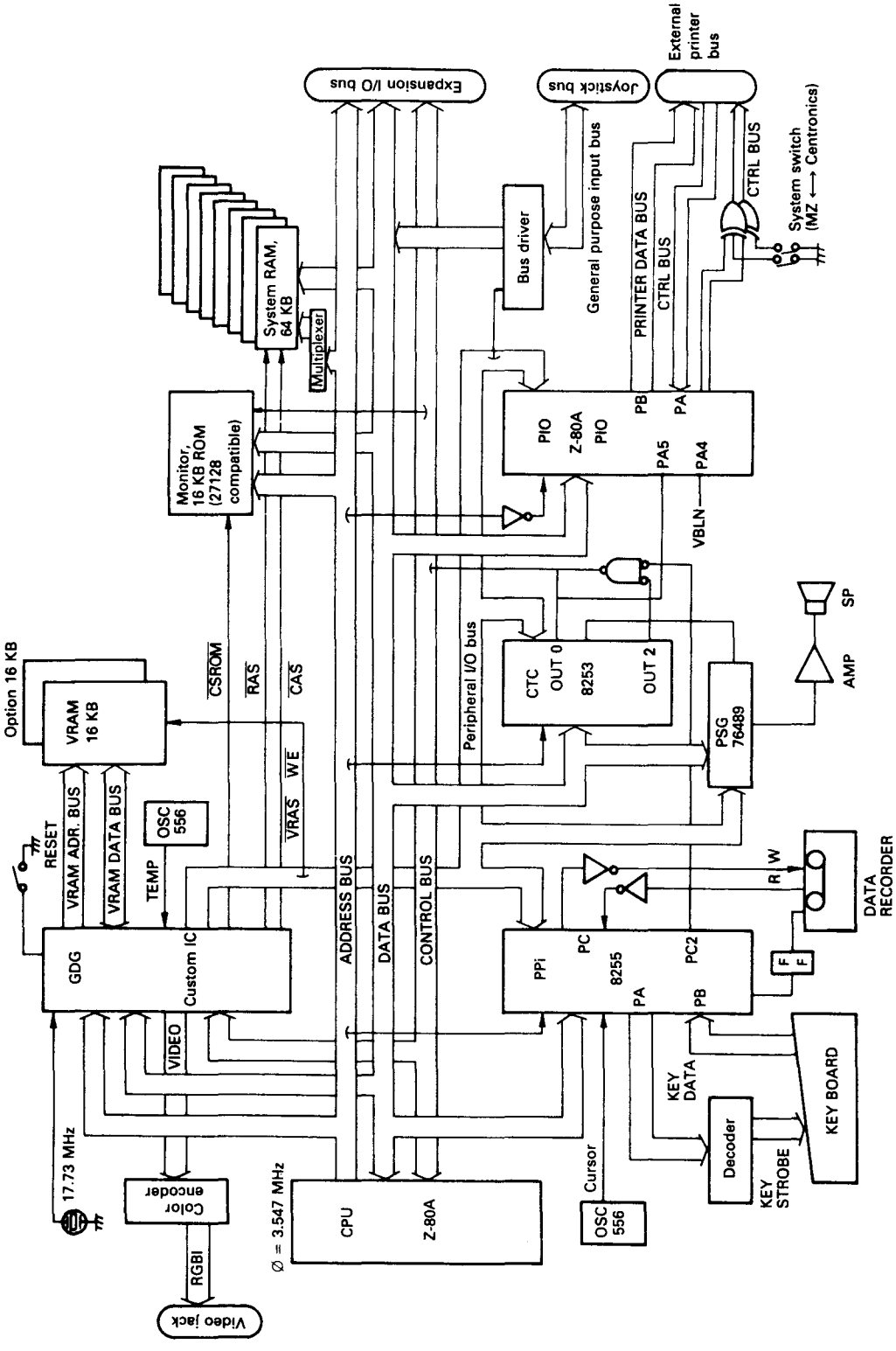
3. System diagram



4. System description

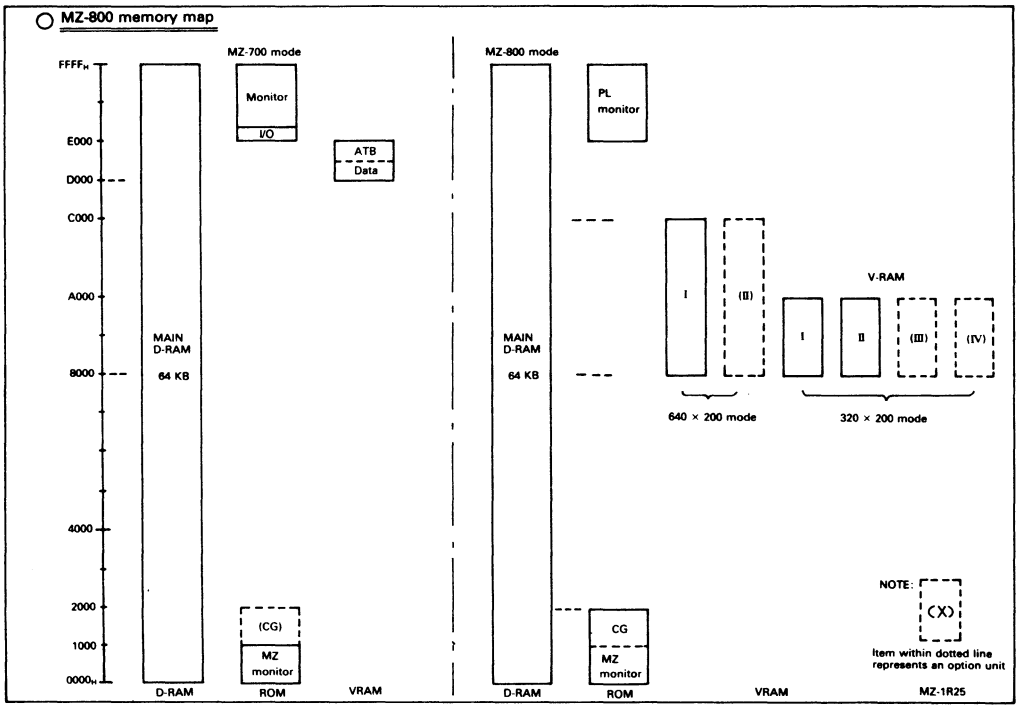


Block diagram

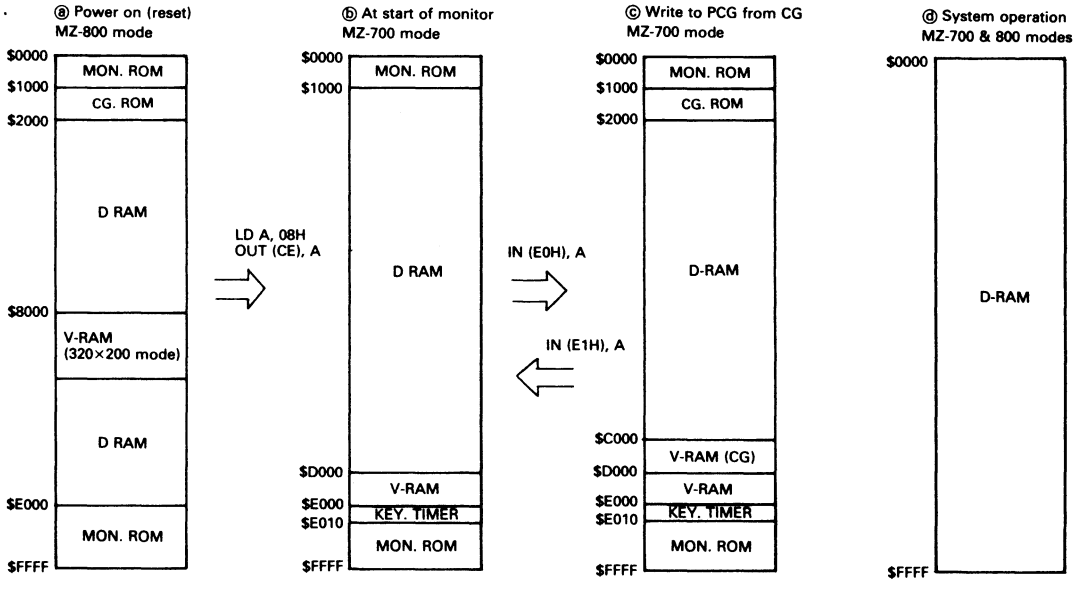


4-1. Memory map

The MZ-800 has a different memory map depending on the mode. To have compatibility with the MZ-700, it has two modes of the MZ-700 mode and MZ-800 mode.



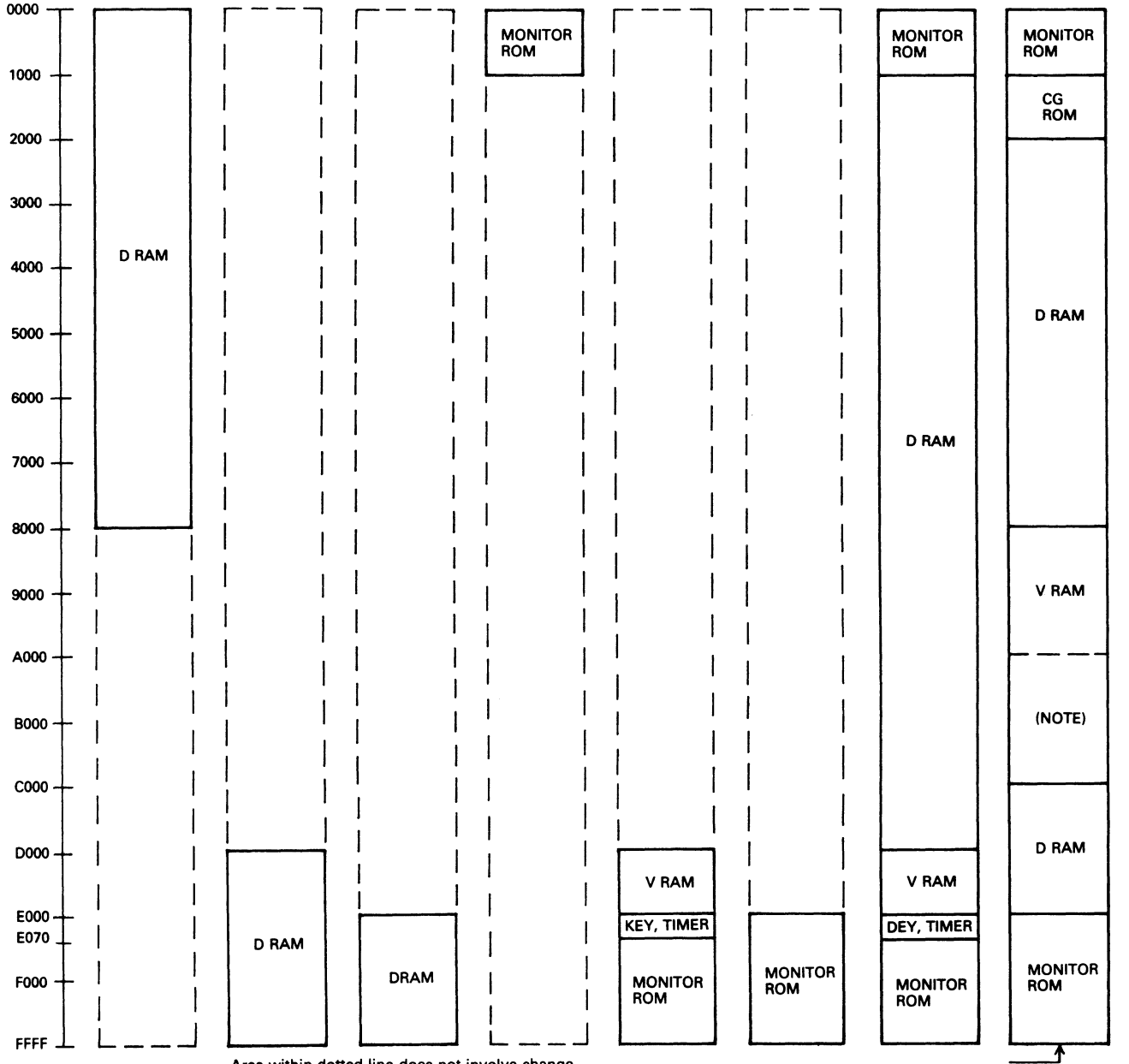
Memory map changes after initial program loading



- Memory map at power on is in the MZ-800 mode as in ⓐ, but it changes to the MZ-700 mode by the monitor ROM when the monitor program starts. After transferring the CG data to the VRAM PCG area from the CG ROM at ⓒ, the memory map then returns to ⓑ.
- When the system program is completed to load, the memory map goes into the MZ-700 mode if the system switch (SW1) is set to ON side. If set to OFF side, it changes to the MZ-800 mode, then the memory map as in ⓓ. During those changes, all memory spaces are composed of RAM and isolated from ROM and VRAM.
- Depression of the manual reset switch assumes memory map transition in order of ⓐ → ⓑ → ⓒ → ⓑ, similar as in the case of power on.
- However, depression of the reset switch in conjunction with the CTRL key assumes the memory map of ⓓ after being changed once to the MZ-700 or MZ-800 mode depending on the state of the system switch. In the case of the MZ-800 mode, it is set to the plane I, II (4-color mode) of the 320 × 200 mode.

Memory Bank Control

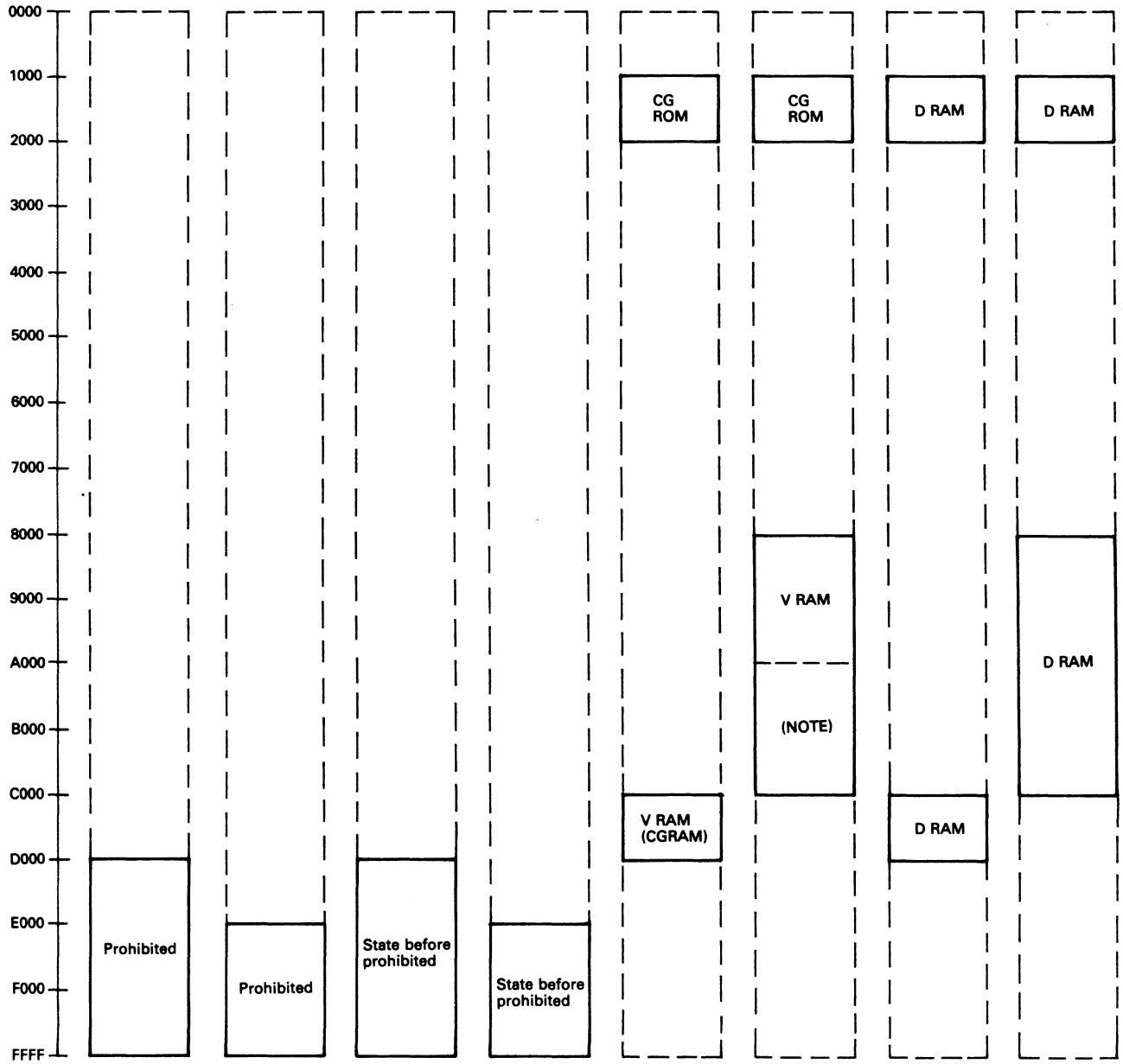
Output port	$E0	$E1		$E2	$E3		$E4	
MODE	—	MZ-700 mode	MZ-800 mode	—	MZ-700 mode	MZ-800 mode	MZ-700 mode	MZ-800 mode
Function	○ $0000 ~ $7FFF to DRAM.	○ $D000 ~ $FFFF to DRAM.	○ $E000 ~ $FFFF to DRAM.	○ $0000 ~ $0FFF to monitor ROM.	○ $D000 ~ $FFFF to VRAM, key timer, and monitor ROM.	○ $E000 ~ $FFFF to monitor ROM.	○ $0000 ~ $0FFF to monitor ROM. ○ $1000 ~ $CFFF to DRAM ○ $D000 ~ $FFFF to VRAM, key timer, and monitor ROM.	○ $0000 ~ $0FFF to monitor ROM. ○ $1000 ~ $1FFF to CG ROM. ○ $2000 ~ $7FFF and $C000 ~ $DFFF to DRAM. ○ $8000 ~ $BFFF to VRAM (NOTE). ○ $E000 ~ $FFFF to monitor ROM.



Area within dotted line does not involve change.

(NOTE): In the case of 320 × 200 mode, contents of $8000 ~ $9FFF are transferred, instead, and those after $A000 are transferred to DRAM.

I/O port	OUT ($E5)		OUT ($E6)		IN ($E0)		IN ($E1)	
MODE	MZ-700 mode	MZ-800 mode	MZ-700 mode	MZ-800 mode	MZ-700 mode	MZ-800 mode	MZ-700 mode	MZ-800 mode
Function	○ $D000 ~ $7FFF prohibited.	○ $E000 ~ $FFFF prohibited.	○ $D000 ~ $FFFF returned to the state before prohibited.	○ $E000 ~ $FFFF returned to the state before prohibited.	○ $1000 ~ $1FFF to CG ROM. ○ $C000 ~ $CFFF to VRAM (PCG RAM).	○ $1000 ~ $1FFF to CG ROM. ○ $8000 ~ $BFFF to VRAM (NOTE).	○ $1000 ~ $1FFF returned to the state before CG was set. ○ $C000 ~ $CFFF to DRAM.	○ $1000 ~ $1FFF returned to the state before CG was set. ○ $8000 ~ $BFFF to DRAM.



4-2. Custom LSI

The custom LSI is a 100-pin single chip LSI on which the MZ-800 memory controller (I/O controller) and CRT controller, etc. are contained.

4-2-1. Memory controller

Used for the control of the memory bank. Addressing of DRAM, ROM, and VRAM is conducted by selection I/O address, $E0 ~ $E6, using OUT or IN command.

4-2-2. I/O controller

In this I/O controller is created the select signal for assignment of MZ-800 internal device.
See Table-2 for relation of internal device vs I/O address.

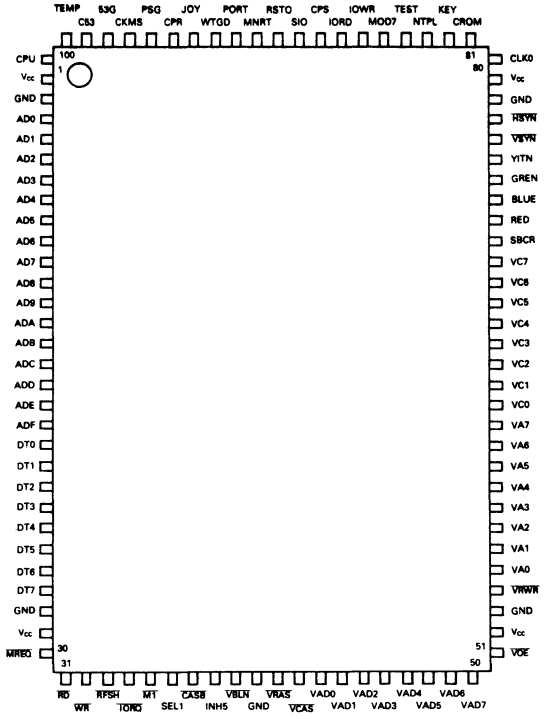
I/O address	Signal name	Device (I/O)	Function
FF FE FD FC	CPR	Z80A PIO (I/O)	Port B, printer data output Port A, printer control and timer interrupt Port B control (Mode 0) Port A control (Mode 3)
F2	PSG	PSG (O)	PSG output port
F1 F0	JOY	JOYSTICK (I)	Joystick-2 input port Joystick-1 input port
F0	——	(O)	Pallet write
E6 ≀ E0	——	—— (I/O)	Memory bank control
D7 D6 D5 D4	C53	8253 (I/O)	Control port output Counter-2 Counter-1 Counter-0 (NOTE): Mapped to E007 ~ E004 in the MZ-700 mode.
D3 D2 D1 D0	KEY	8255 (I/O)	Control Port C, cassette, etc. Port B, key input Port A, key strobe output (NOTE): Mapped to E003 ~ E000 in the MZ-700 mode.
CF CE CD CC	——	—— O I/O O O	CRTC register
$E008	——	—— I/O	TEMP, HBLK input; and 8253 G0 ON/OFF output for the MZ-700 mode only.

* When above I/O address is accessed, it makes IOWR active for OUT or IORD for IN command.

Pin No.	Signal name	I/O	Functional description	Note
1	CPU	O	CPU clock (3.547 MHz)	
2	5 V	—	Power supply	
3	GND	—	Ground	
4 ~ 19	AD0 ~ ADF	I	CPU address bus	
20 ~ 27	DT0 ~ DT7	I/O	CPU data bus	
28	GND	—	Ground	
29	VCC	—	Power supply	
30	$\overline{\text{MREQ}}$	I	CPU $\overline{\text{MREQ}}$ signal	Negative logic
31	$\overline{\text{RD}}$	I	CPU $\overline{\text{RD}}$ signal	Negative logic
32	$\overline{\text{WR}}$	I	CPU $\overline{\text{WR}}$ signal	Negative logic
33	$\overline{\text{RFSH}}$	I	CPU $\overline{\text{RFSH}}$ signal	Negative logic
34	$\overline{\text{IORQ}}$	I	CPU $\overline{\text{IORQ}}$ signal	Negative logic
35	$\overline{\text{M1}}$	I	CPU $\overline{\text{M1}}$ signal	Negative logic
36	SEL1	O	System RAM address multiplexer select signal	
37	CASB	O	System RAM column address strobe signal	
38	INH5	O	Inhibit bank (OUT $E5) select signal ("H" = Inhibit).	OPEN
39	$\overline{\text{VBLN}}$	O	Vertical blanking signal	Negative logic
40	GND	—		
41	$\overline{\text{VRAS}}$	O	VRAM RAS control signal	Negative logic
42	$\overline{\text{VCAS}}$	O	VRAM CAS control signal	Negative logic
43 ~ 50	VAD0 ~ VAD7	O	VRAM address signal (multiplexer output)	
51	$\overline{\text{VOE}}$	O	VRAM output enable	Negative logic
52	VCC	—	Power supply	
53	GND	—	Ground	
54	$\overline{\text{VRWR}}$	O	VRAM write signal	Negative logic
55 ~ 62	VA0 ~ VA7	I/O	VRAM data bus (standard RAM)	
63 ~ 70	VC0 ~ VC7	I/O	VRAM data bus (option RAM)	
71	SBCR	O	Color sub-carrier wave	
72	RED	O	Video signal, red	
73	BLUE	O	Video signal, blue	
74	GREN	O	Video signal, green	
75	YITN	O	Brightness control signal	
76	$\overline{\text{VSYN}}$	O	Vertical sync signal	Negative logic
77	$\overline{\text{HSYN}}$	O	Horizontal sync signal	Negative logic
78	GND	—		
79	VCC	—		
80	CLK0	I	Clock input (17.7344 MHz)	
81	$\overline{\text{CROM}}$	O	ROM chip enable	Negative logic
82	$\overline{\text{KEY}}$	O	8255 chip enable	Negative logic
83	NTPL	I	NTSC/PAL selection (PAL = "L")	GND
84	TEST	I	Test pin ("H" = test mode)	GND
85	MOD7	I	MZ-700/800 mode selection ("L" = MZ-700 mode)	
86	$\overline{\text{IOWR}}$	O	Sum of CS and WR of I/O controlled by the custom IC	Negative logic
87	$\overline{\text{IORD}}$	O	Sum of CS and RD of I/O controlled by the custom IC	Negative logic
88	CRS	O	I/O $B0 ~ $B4 chip enable	OPEN
89	SIO	O	I/O $F4 ~ $F7 chip enable	OPEN
90	$\overline{\text{RSTO}}$	O	Reset output	Negative logic
91	$\overline{\text{MNRT}}$	I	Manual reset input	Negative logic
92	$\overline{\text{PORT}}$	I	Power on reset input	Negative logic
93	WTGD	O	Wait signal to CPU	Open drain
94	$\overline{\text{JOY}}$	O	Joystick chip enable	Negative logic
95	$\overline{\text{CPR}}$	O	PIO chip select	Negative logic
96	$\overline{\text{PSG}}$	O	76489 chip select	Negative logic
97	CKMS	O	8253 musical interval clock	
98	53G	O	8253 musical interval ON/OFF gate signal	
99	$\overline{\text{C53}}$	O	8253 chip enable	Negative logic
100	TEMP	I	MZ-700 mode, $E800 tempo input	

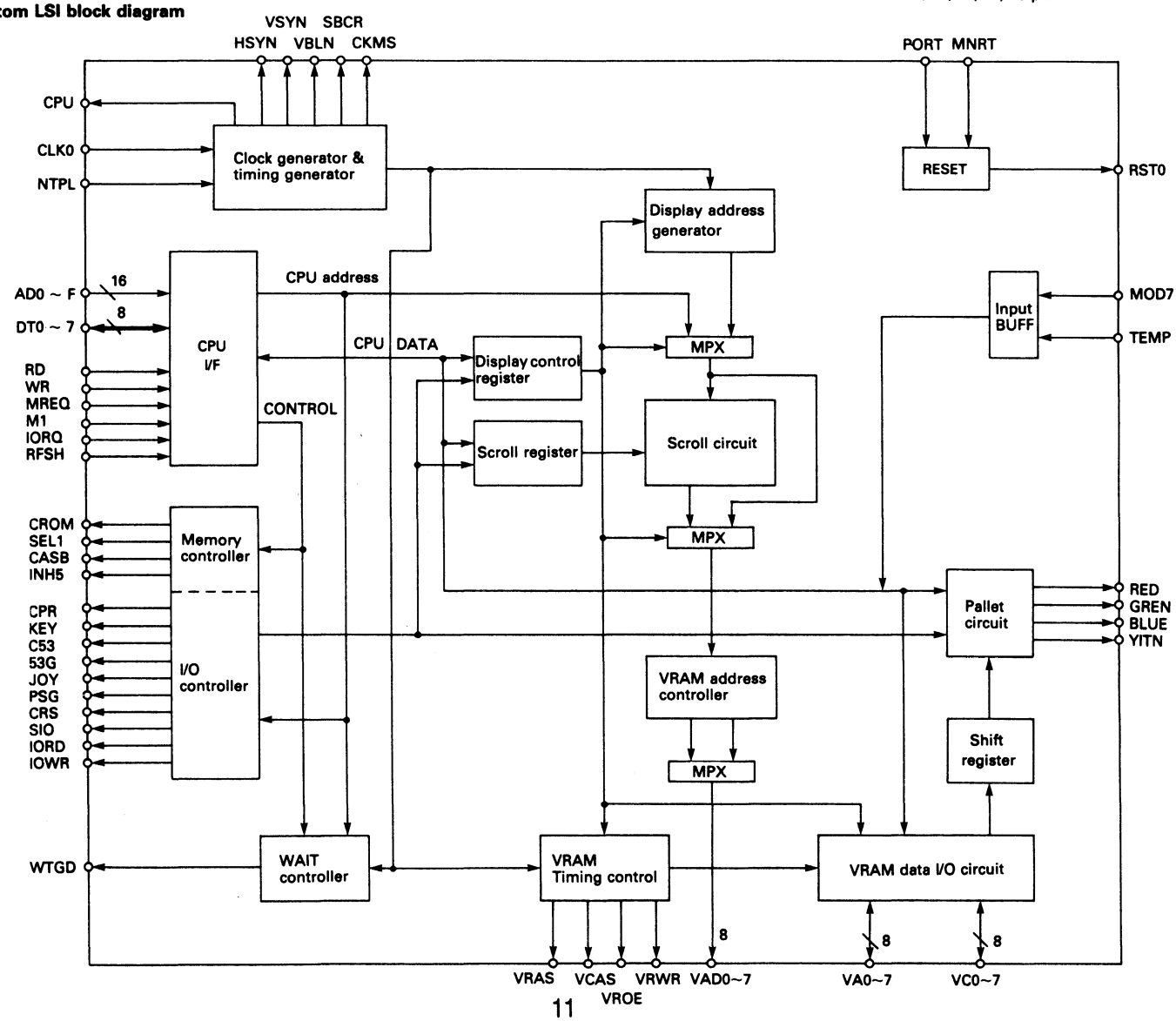
* Term "OPEN" represents the signal not used on the board.

Pin configuration



V_{CC} 2, 29, 52, 79, pin
GND 3, 28, 40, 53, 78 pin

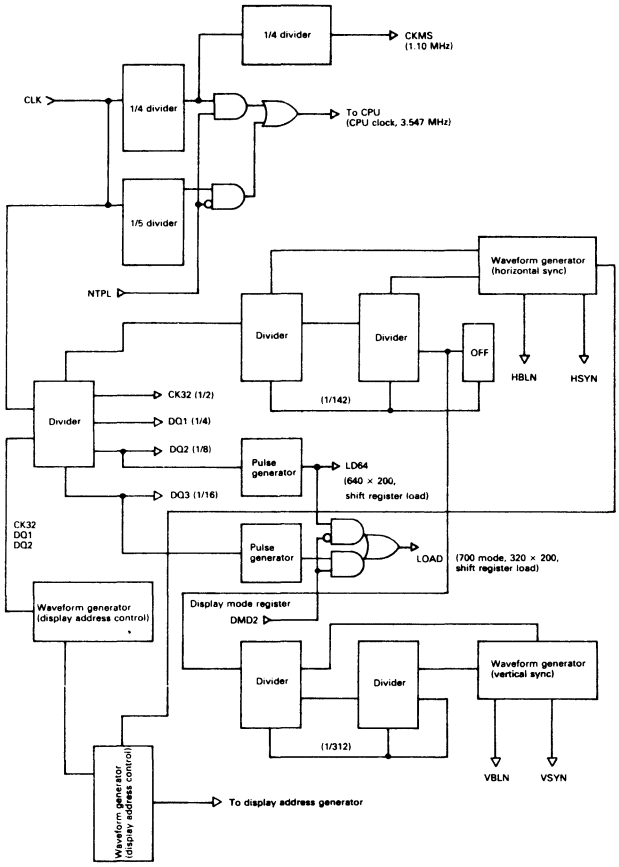
Custom LSI block diagram



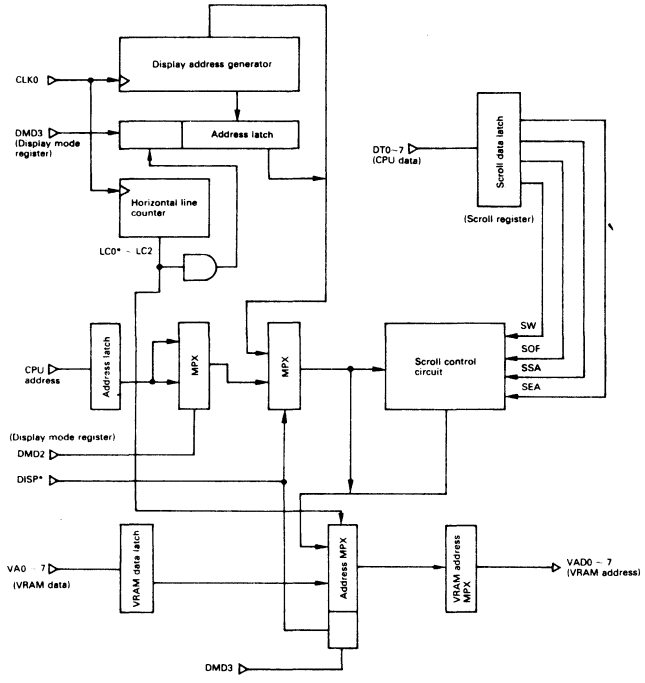
4-2-3. Clock generator and timing generator

Oscillation from the crystal oscillator is divided to create the CPU clock, horizontal sync, vertical sync, and display address control signals.

Since the low state of signal is used for NTPL (NTSC/PAL selection) with the MZ-800, the CPU clock of 3.547 MHz is derived from the crystal frequency of 17.734 MHz by dividing it 1/5.



Clock generator and timing generator circuits



Display address generator block diagram

4-2-4. Display address generator

1) Display address generation

- Display address increments from left to right as beginning from the home position at the upper left corner of the CRT screen (address $000). The first display line dominates address $000 through $027. Because a screen frame consists of 200 rasters, the address at the right side of the bottom corner is as follows:

  $(200 \times 40) - 1 = 7999 = \$1F3F$

- The address counter stops counting for a horizontal flyback line and stored in the address latch circuit. When the horizontal flyback line terminates, the address latch output is preset in the address counter (display address generator).
- Address is generated even while the vertical flyback line is active and it makes the counter reset before termination of the vertical flyback line.

2) Display address generation in the MZ-700 mode

- Because characters are displayed under the PCG method in the MZ-700 mode, address is generated for each character and the same address is used for displaying of one character. The 3-bit horizontal line counter is provided to count horizontal lines to generate the address (LC0 ~ LC2) for selection of the character front.

  Display address increments from left to right having the uppermost left corner of the screen for the home position.

  Since 25 lines are used to develop displaying of characters composed of 8 × 8 dots, the address at the right of the bottom lines becomes $3EF.

3) Display address multiplexed with CPU address

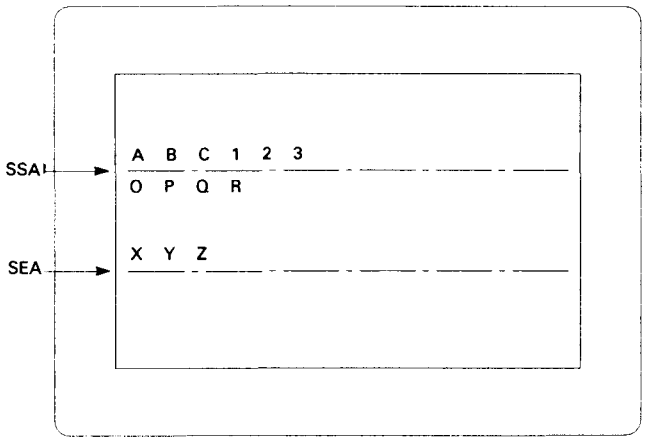
- Address used to write data to the VRAM is latched in order to avoid CPU wait. Display modes of 640 dots and 320 dots are assigned by the mode switch (DMD2).
- Display address is multiplexed with the VRAM write address in the timing of DISP which has the timing that the display address and CPU address may become a pseudo cycle steal.

4-2-5. Scroll

1) Scrolling is possible for both horizontal and vertical directions by means of software offset.

The following four registers are used for scroll control.

a. Scroll start address register: SSA (7-bit)
b. Scroll end address register: SEA (7-bit)
c. Scroll width register: SW = SEA-SSA (7-bit)
d. Scroll offset register: SOF (10-bit)



2) Control of scroll starts by the initialization of the scroll control register.

SSA = $0
SEA = $7D
SW = $7D
SOF = $0

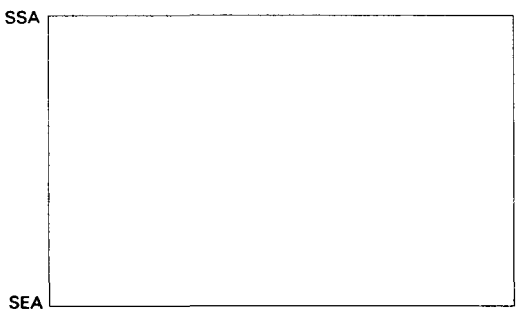
3) Way of smooth scrolling

SOF = $0 → $5

Programming "SOF = $5" makes the display screen shifted one line up.
The highest line (address: $0 ~ $27) is then assigned to the lowest line ($1F18 ~ $1F3F).
As normal scroll involves updating of the data for the lowest line, the data of address $1F18 ~ $1F3F are updated.

SOF = $5 → $0

By reducing the value of SOF by "5", it makes the screen shifted one line down.



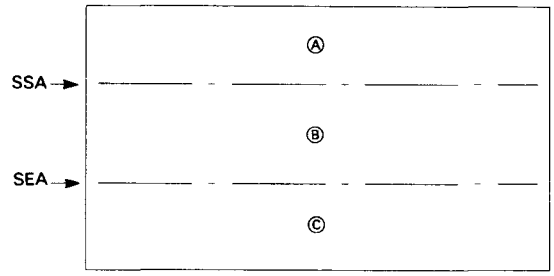
4) Line scroll

SOF = $0 → $28

Programming "SOF = $28" makes the display screen shifted eight lines up. Data on the highest line therefore shifted to the bottom line.
Programming "$28 → $0" makes the display screen shifted eight lines down, and the line on the bottom moves to the highest line.

5) Screen split

Appropriate deviation of SSA, SEA, and SW permits to divide the screen into three sections of Ⓐ, Ⓑ and Ⓒ.
Though the section Ⓑ is permitted to scroll, sections Ⓐ and Ⓒ are not permitted to scroll.
See the figure to explain with.



Assume now that the top of the section Ⓑ is on the 5th line (40 raster) and the top of the section Ⓒ is on the 18th line (144 raster). Attention must be paid to the fact that values SSA and SEA are used for assigning lines. Scroll registers are set with the following values.

SSA = $19
SEA = $5A
SW = $41
SOF = $0

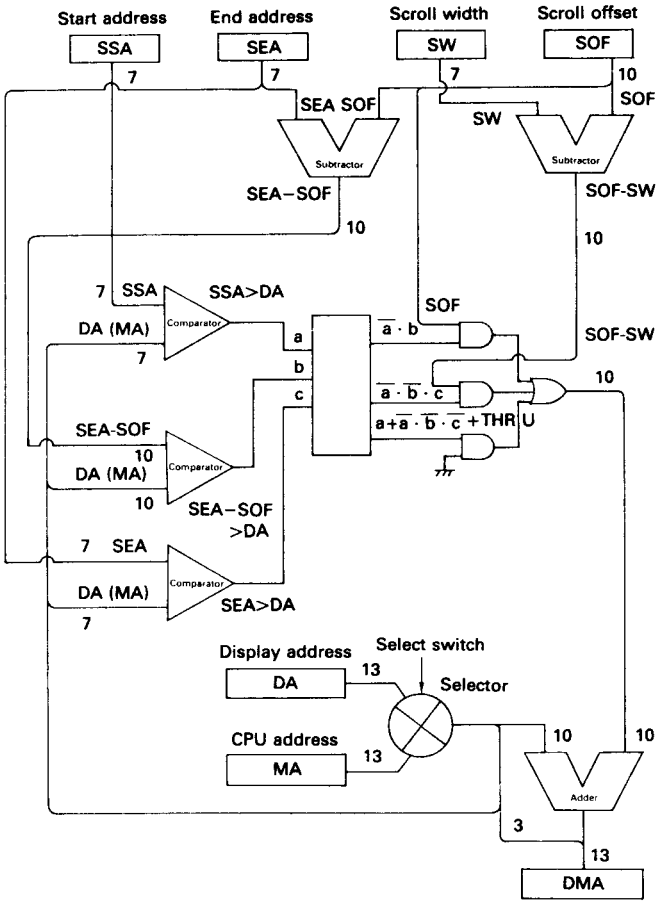
In this occasion, it needs to initialize the screen that has been displayed. "SOF = $5" must be programmed to scroll Ⓑ one line. Then, only the section Ⓑ is shifted up, and the highest line of Ⓑ moves to the bottom line of Ⓑ. Programming "SOF = $A" makes it scrolled one more line.

SOF ≦ SW

Scroll offset (SOF) should necessarily be within a range of the scroll width. Display is not assured with SOF set greater than SW.

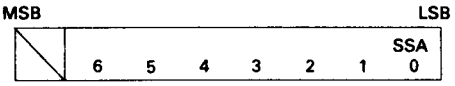
Scroll and and control circuit hardware

- **Block diagram**

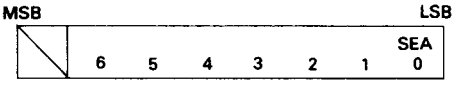


Scroll control register

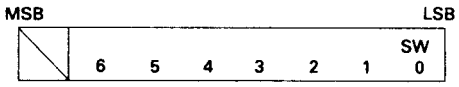
SSA: Scroll start address
Increment of SSA: $5
Minimum value of SSA: $0
Maximum value of SSA: $78



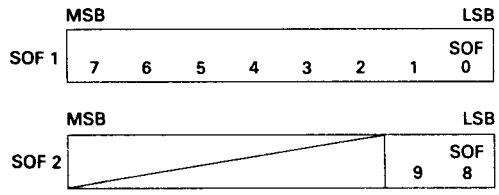
SEA: Scroll end address
Increment of SEA: $5
Minimum value of SEA: $5
Maximum value of SEA: $7D



SW: Scroll width
Increment of SW: $5
Minimum value of SW: $5
Maximum value of SW: $7D
Relation of SW, SEA, vs SSA
SW = SEA − SSA
SW > SSA



SOF: Scroll offset
Increment of SOF: $5
Minimum value of SOF: $0 (without offset)
Maximum value of SOF: $3E8



Relation of display address, SEA, SSA, vs SOF

Display address	m	l	k	j	i	h	g	f	e	d	c	b	a	
SSA	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	–	–	–	–	–	–	
SEA	SEA 6	SEA 5	SEA 4	SEA 3	SEA 2	SEA 1	SEA 0	–	–	–	–	–	–	
SOF	SOF 9	SOF 8	SOF 7	SOF 6	SOF 5	SOF 4	SOF 3	SOF 2	SOF 1	SOF 0				
Screen left end address														
0 Line	0	0	0	0	0	0	0	0	0	0	0	0	0	
1 Line	0	0	0	0	0	0	0	1	0	1	0	0	0	First line
2 Line	0	0	0	0	0	0	1	0	1	0	0	0	0	
3 Line	0	0	0	0	0	0	1	1	1	1	0	0	0	
8 Line	0	0	0	0	1	0	1	0	0	0	0	0	0	Second line
16 Line	0	0	0	1	0	1	0	0	0	0	0	0	0	Second line
24 Line	0	0	0	1	1	1	1	0	0	0	0	0	0	
192 Line	1	1	1	1	0	0	0	0	0	0	0	0	0	Twenty fifth line
199 Line	1	1	1	1	1	0	0	0	1	1	0	0	0	

Relation of SW vs SOF

SW > SOF

Concept of the scroll control circuit

Scroll method

- Scrolling by means of VRAM address conversion.

Range of scroll

- y-axis programmable.
  BASIC console command compatible
- x-axis fixed

Scroll sequence

- The scroll start address is termed "SSA" and end address "SEA".
- Execution of scroll, with offset given from the CPU.
- One line (line S) starting from SSA disappears from the display screen.
- A new line (line S') is added to SEA. Line S' is the same refresh memory as the line S. The contents of the memory was erased (nullified by the CPU) before the execution.

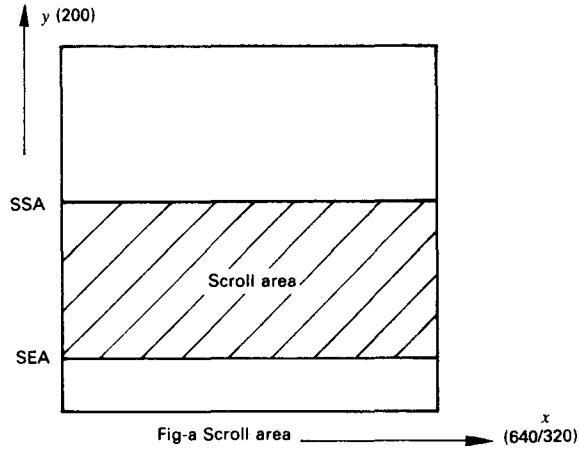


Fig-a Scroll area

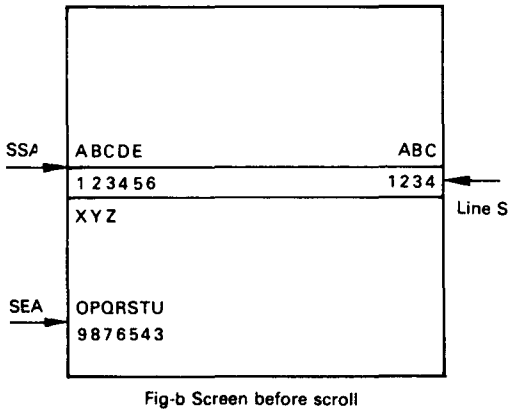


Fig-b Screen before scroll

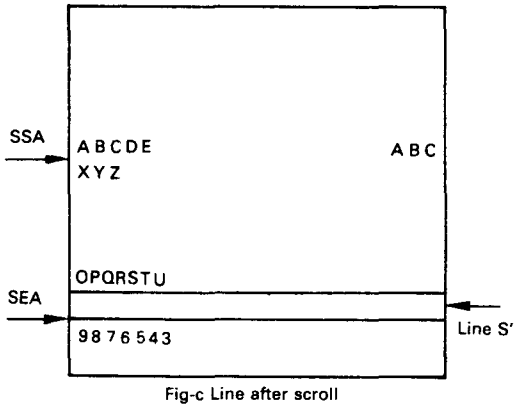
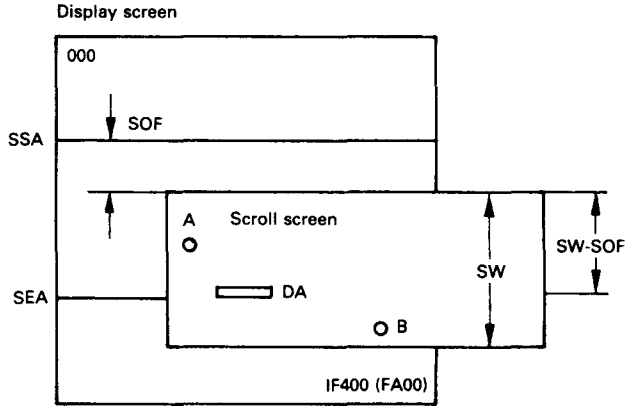


Fig-c Line after scroll

Execution of scrolling by address conversion

- Scroll offset (SOF) is the count of lines which the CPU gives to the CRTC. For instance, the following must be observed to perform scrolling.
  3-line scroll: $SOF_3 = 0F \times 3$
  5-line scroll: $SOF_5 = 0F \times 5$
  And, to scroll one more line after 5-line scroll;
  5-line scroll: $SOF_5' = SOF5 + 0F = OF \times 6$



- Display address DA is the signal created in the CRTC display address generation circuit and arranged in their order from the upper left corner of the screen. The bottom right address is 1F400 in the 640 × 200 mode.
- Display memory address DMA represents the VRAM address corresponding to DA.
  Since scroll is executed by means of address conversion, the order of DMA may not be the same as DA, necessarily.
- CPU address MA is the VRAM address that obtained from the CPU through the CRTC. To lighten burden on the CPU, a circuit is added to make order of DA identical to order of MA arrangement.

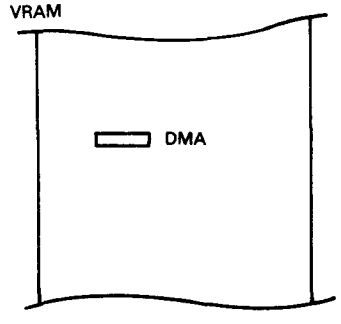


Fig-d Address conversion

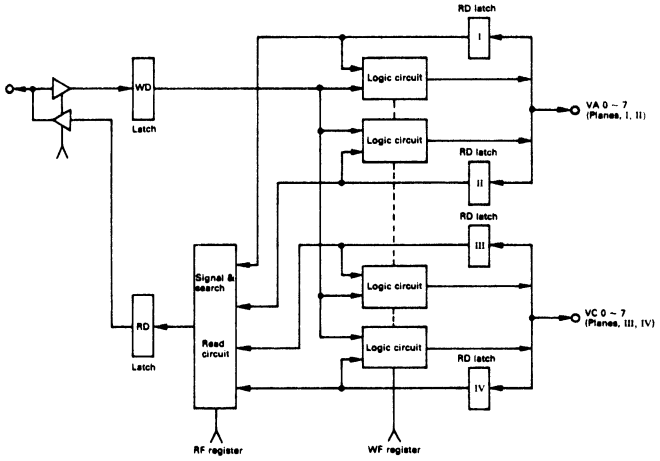
4-2-6. VRAM data input/output circuit

1. Nothing intervenes for input and output of data in the case of the MZ-700 mode.
2. MZ-800 mode

- Write
  Read data (RD) from the VRAM and write data (WD) from the CPU are subjected to logical operation according to the direction from the write format register (WF) and its result is written.

- Read

  For plane read data from the VRAM, data to be read by the CPU are arranged in accordance with the direction of the read format register (RF).



* Logic circuit

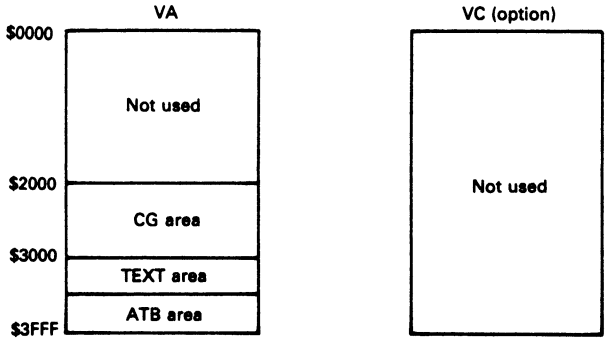
Read data from the VRAM and write data from the CPU are subjected to logical operation (OR, XOR, RESET, etc.) and its result is used for the write data.

VRAM access timing

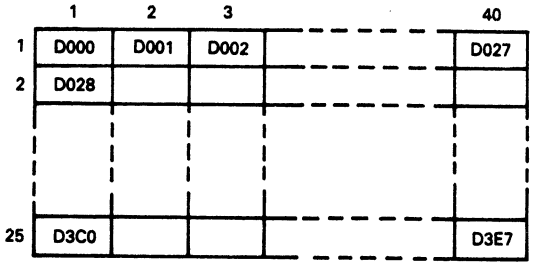
1) MZ-700 mode

See separate page for display timing chart.

The VRAM is configured in the following manner in this instance.



As the PCG method is adopted for the MZ-700 mode, the text and ATB areas are actually mapped to $D000 ~ $DFFF. So, the VRAM address has the following relation with the display character position.



2) MZ-800 mode

As the bit map method is used for the MZ-800 mode, it is possible to four screens of 320 × 200 dots and two screens (maximum) of 640 × 200 dots.

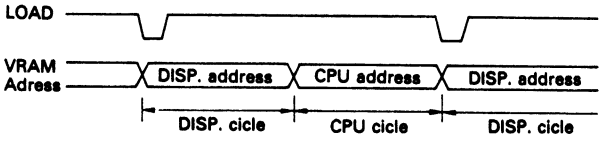
The cycle steal method is used for this mode.

i) 320 × 200 dots

See separate page for the timing chart during display and CPU read timing.

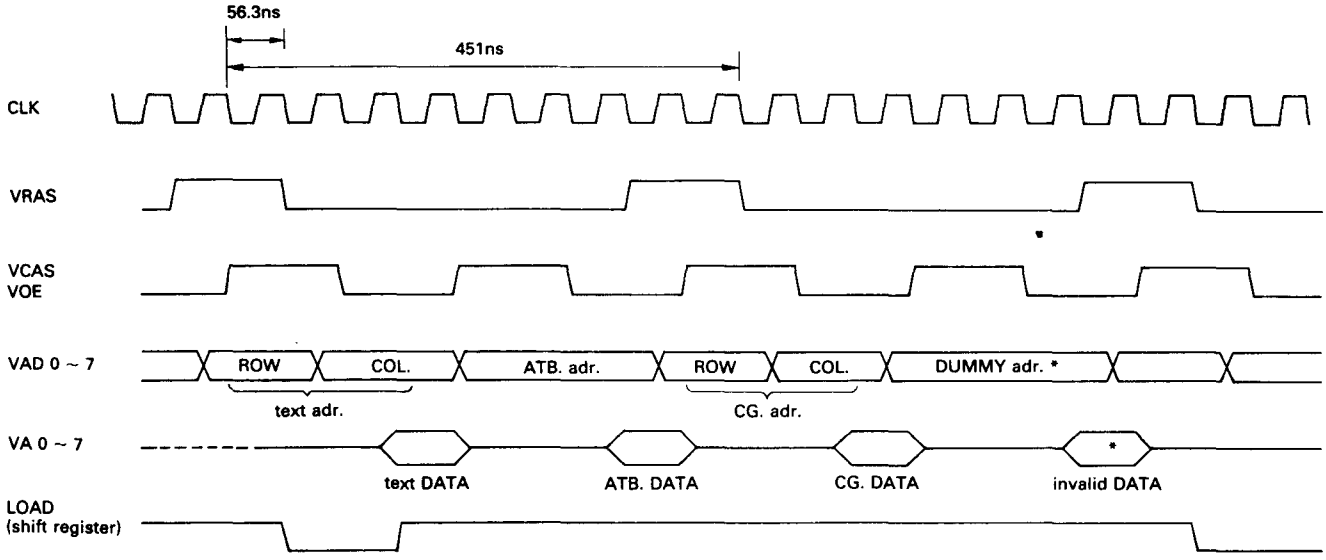
What is pseudo cycle steal

With the MZ-800, the pseudo cycle steal method is adopted for VRAM accessing.

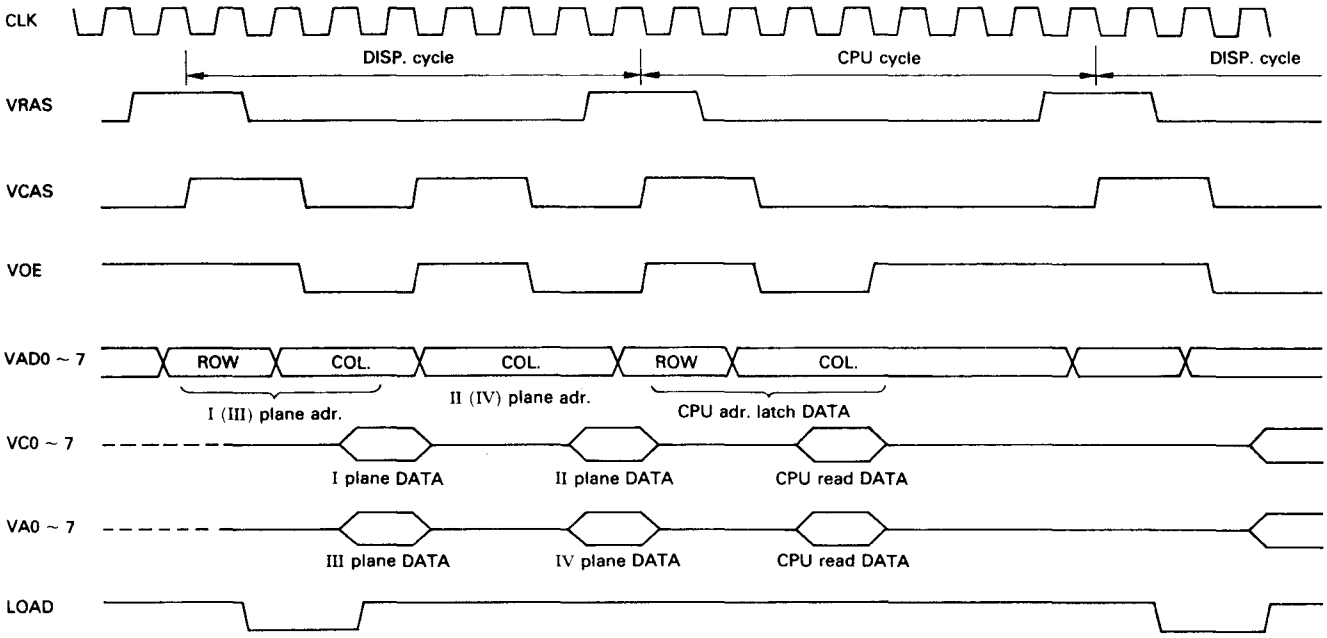


As shown in the figure, a next display data fetch and CPU accessing are multiplexed during a display period. Because accessing of the VRAM while characters are on display causes the screen to blink with the MZ-700 mode, it awaits for blinking to complete before accessing of the VRAM. But, with the cycle steal method it enhances faster screen processing as it enables to access the VRAM during a display period. Because it is not a complete cycle steal with the MZ-800 but timing is taken using a wait in order to synchronize with the CPU cycle for accessing from the CPU, it is therefore called "pseudo cycle steal".

MZ-700 MODE DISPLAY TIMING

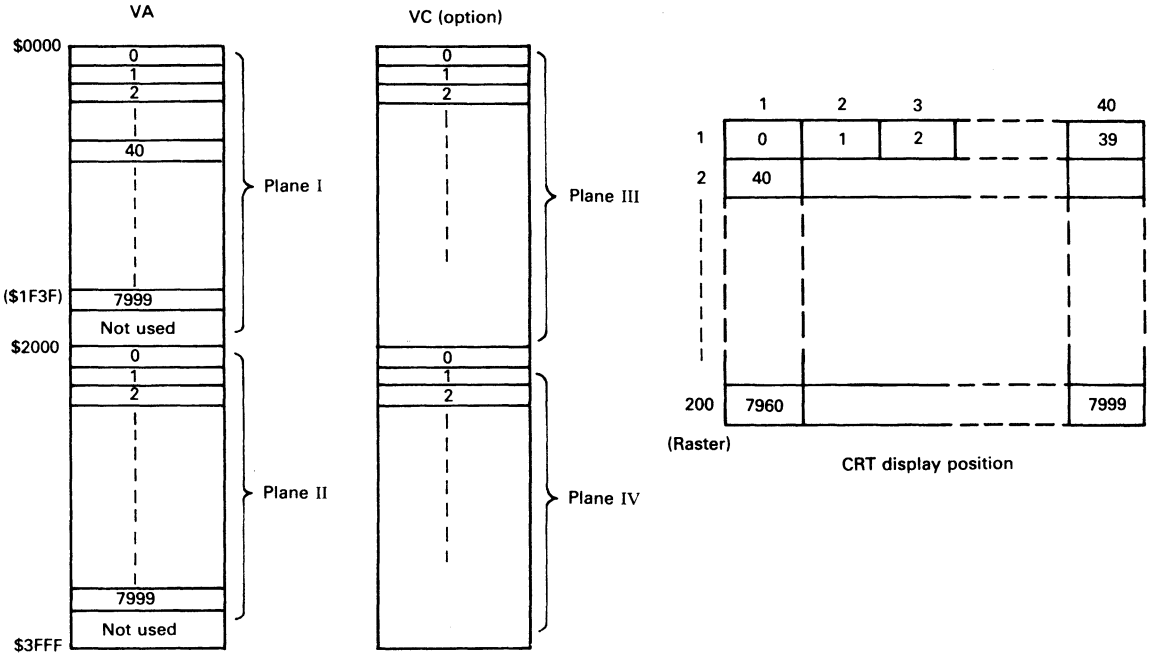


MZ-800 MODE (320 × 200 dot)



1) 320 × 200 dots

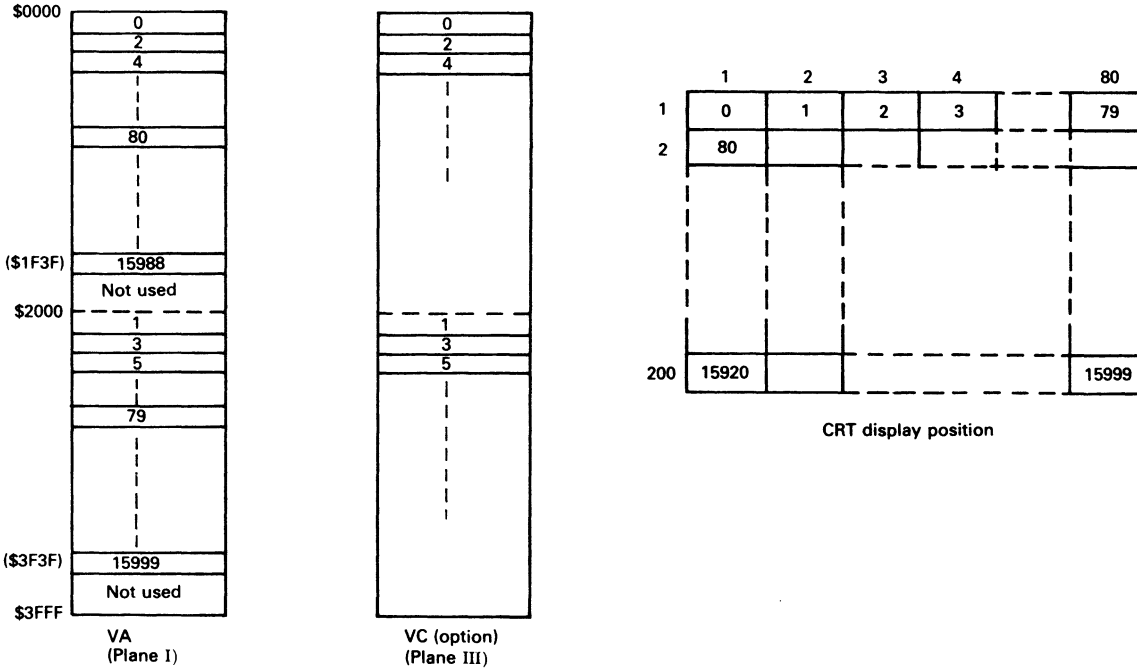
See the figure below for VRAM configuration and CRT character display position.



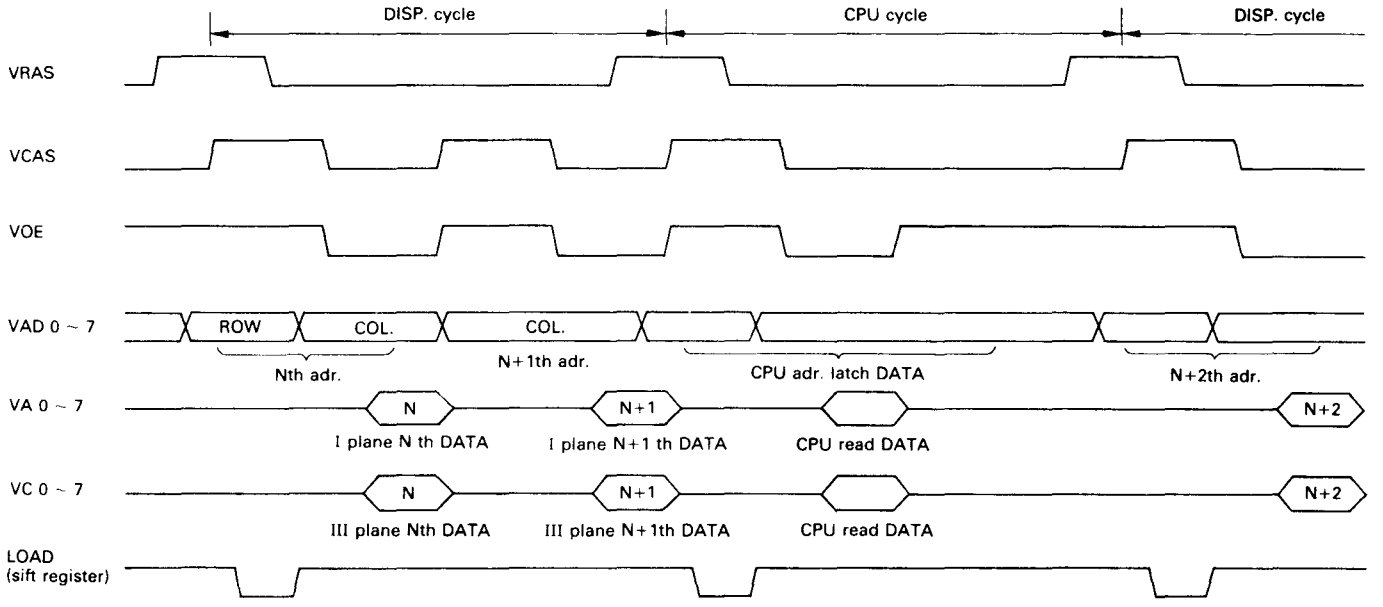
2) 640 × 200 dots

Because it operates in the cycle steal mode, two bytes of display data are fetched during one byte display cycle. (See the chart in separate page.)

See the figure below for VRAM configuration and CRT character display position.



800 MODE (640 × 200 dot)

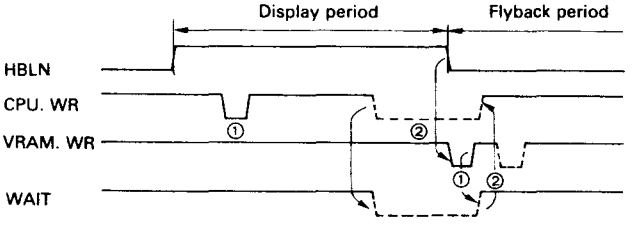


CPU and VRAM accessing

1. Accessing of the VRAM by the CPU is carried out in the cycle steal mode (MZ-800 mode only) during the flyback period of the display under the control of the CRT controller.
2. Even when there is no accessing from the CPU in the CPU cycle, such as VRAS, VCAS, VOE, etc. are outputted in the timing of the read cycle at all times.
3. Write to the VRAM is carried out after logical operation of the read and write data by means of the read-modify-write method. But, in the case of the 320 × 200, 16-color mode, data are written in two CPU cycles as there is a need of writing to Plane IV.
   See separate paper for timing chart.
4. CPU wait

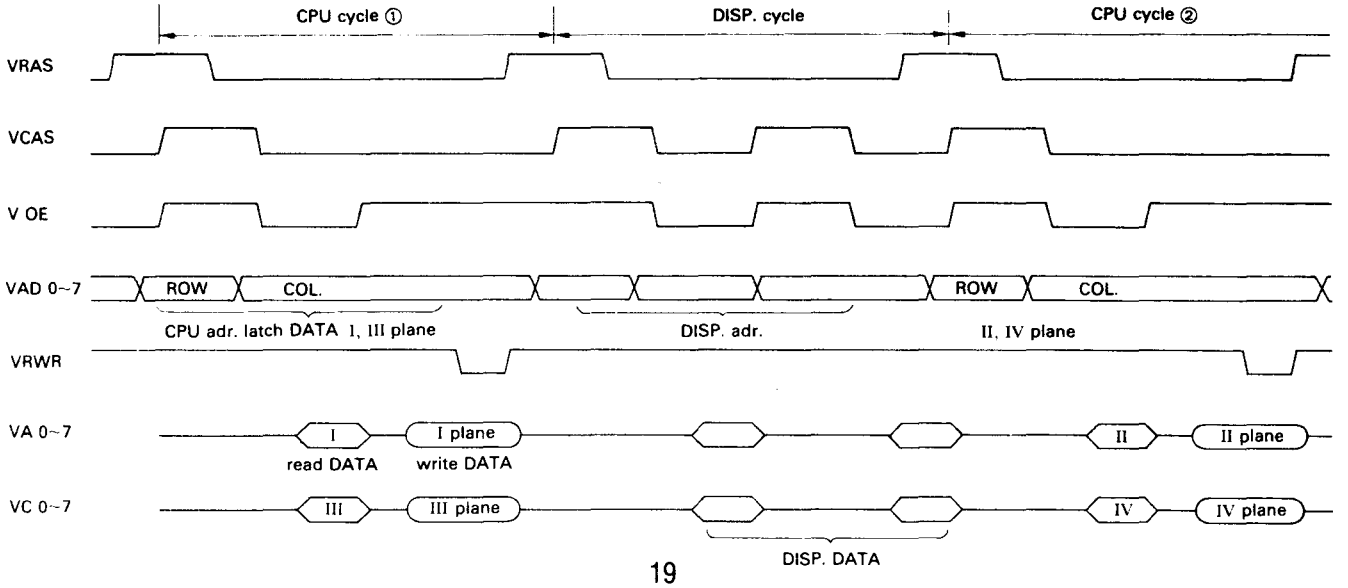
1) Write

- As there is a one-byte buffer in the CRT controller, write to the VRAM from the CPU is carried out through the buffer. But, actual write to the VRAM is done by the CRT controller. Therefore, there would be no need of wait under almost any condition in the MZ-800 mode.
- Even in the MZ-700 mode, wait is issued when there are more than two writes in a display period.



2) Read

Wait is issued along with the CPU write action both during displaying and flyback periods to perform reading operation in synchronization with the CPU cycle.



4-2-7. Register functions

VRAM configuration

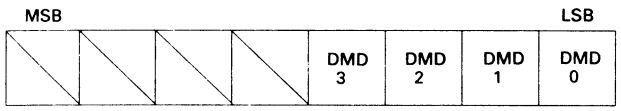
- One or two chips of 16 KB VRAM are used.
- In the case of a single 16 KB VRAM chip, it handles 320 × 200 dots, 4 colors, or 640 × 200 dots 1 color.
- In the case of two 16 KB VRAM chips, it handles 320 × 200 dots, 16 colors, 640 × 200 dots, 4 colors, 320 × 200 dots, 4 colors, 2 frames, or 640 × 200 dots, 1 color, two frames.

* Discussed next are about functions of the custom LSI. There may be some restrictions because the standard version of the MZ-800 incorporates only one 16 KB RAM.

Display mode register (OUT &HCE)

- It consists of four bits which are used to represent display method, resolution, and display screen (color plane) in combined way.

Display mode register (DMD)



- DMD 3, 2: Display method and resolution

DMD 3	2	
0	0	Bit map, 320 × 200
0	1	Bit map, 640 × 200
1	0	MZ-700 mode
1	1	Prohibited

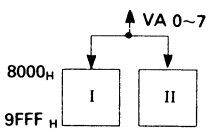
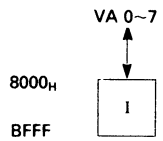
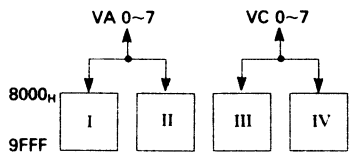
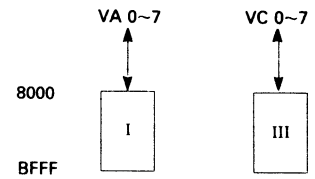
- DMD 1, 0: Display screen designation

DMD 1	DMD 0	320 × 200	640 × 200	MZ-700
0	0	Frame A, Planes I and II	Frame A, Plane I	Normal
0	1	Frame B, Planes III and IV	Frame B, Plane III (NOTE)	Prohibited
1	0	Planes I, II, III, and IV	Planes I, III	Prohibited
1	1	Prohibited		

NOTE: 640 × 200, Plane B is Plane III, not Plane II. ⚠ 3/3

* With the MZ-800, DMD 1 = 0, DMD 0 = 0.

Table-1 VRAM configuration and display mode

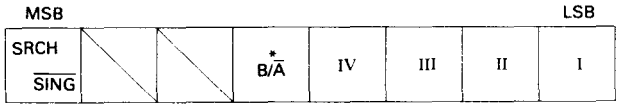
VRAM capacity	VRAM configuration	Resolution	Display color	Display frame	Color combination (NOTE)	DMD 3	2	1	0
16 KB		320 × 200	4 colors	Frame A	I, II	0	0	0	0
		640 × 200	1 color	Frame A	I	0	1	0	0
32 KB		320 × 200	4 colors	Frame A	I, II	0	0	0	0
				Frame B	III, IV	0	0	0	1
			16 colors	Frame A	I, II, III, IV	0	0	1	0
		640 × 200	1 color	Frame A	I	0	1	0	0
				Frame B	III	0	1	0	1
			4 colors	Frame A	I, III	0	1	1	0
	MZ-700	40 characters × 25 lines	8 colors	Frame A	RGB	1	0	0	0

(NOTE) Except for the MZ-700 mode, actual display colors are produced by the pallet.

VRAM to CPU interface

- As the CRTC bus is completely separated from the CPU bus, read and write of the VRAM is carried out through the CRTC. Therefore, interfacing with the CPU is done via the read register or write register in the CRTC.
- VRAM access by the CRTC is done under the pseudo cycle steal mode.
- Not only read and write are for the accessing with the CPU, it permits to read multiple number of screen data logical operational results and to write the read-modify-write of the logical operational results for the data already written. So, it has two registers of the read format register and the write format register.
- It permits CPU access to the non-display plane in the display mode according to the B/$\overline{A}$ bit and it enables selection of data buffer and two screens, when the 32 KB VRAM is used.

a) Read format register (RF) (OUT & CD)



* NOTE: Same as the bit B/$\overline{A}$ of the write format register.

- SRCH/$\overline{SING}$

"0": Single color data read .....

Reads the data of the color plane, I, II, III, or IV, specified by "1".

NOTE: Only one item should be "1" out of I, II, III, and IV. If it is "1" for more than two or non-existence of the VRAM may not assure the data read.

"1": Specified color search .....

"1" is returned for the bit of the color specified by 0/1 of I, II, III, and IV.

NOTE: Depending on the display more, color combination is permitted for the bit combination of I, II, III, IV; III, IV; I, II; I; and III. Bit combination otherwise will be disregarded.

(ex. For the 640 × 200, 4-color mode, combination becomes possible for I and III, and II and IV are disregarded.

- B/$\overline{A}$

CPU access plane change

MZ-800 → "0": Frame A access .....

Accesses the frame A (planes I and II for the 320 × 200, 4-color mode; plane I for the 640 × 200, 1-color mode).

"1": Frame B access .....

Accesses the (planes III and IV for the 320 × 200, 4-color mode; plane II for the 640 × 200, 1-color mode).

- I, II, III, IV ..... Color plane designation.

Table-2 Display mode vs read format register

	Display mode	SRCH/$\overline{SING}$	B/$\overline{A}$	IV	III	II	I	Function (NOTE)
Single color data read	320 × 200, 4/16 colors 640 × 200, 1/4 colors	0	(*) Frame A: "0" Frame B: "1"	0	0	0	1	Plane I data read
				0	0	1	0	Plane II data read
				0	1	0	0	Plane III data read
				1	0	0	0	Plane IV data read
Specified color search	320 × 200, 4 colors	1	0	×	×	0	0	$\overline{I}$, $\overline{II}$ dot search
				×	×	0	1	I, $\overline{II}$ dot search
				×	×	1	0	$\overline{I}$, II dot search
				×	×	1	1	I, II dot search
			1	0	0	×	×	$\overline{III}$, $\overline{IV}$ dot search
				0	1	×	×	III, $\overline{IV}$ dot search
				1	0	×	×	$\overline{III}$, IV dot search
				1	1	×	×	III, IV dot search
	320 × 200, 16 colors	1	×	0	0	0	0	$\overline{I}$, $\overline{II}$, $\overline{III}$, $\overline{IV}$(, dot search
				0	0	0	1	I, $\overline{II}$, $\overline{III}$, $\overline{IV}$(, dot search
				0	0	1	0	$\overline{I}$, II, $\overline{III}$, $\overline{IV}$, dot search
				0	0	1	1	I, II, $\overline{III}$, $\overline{IV}$, dot search
				0	1	0	0	$\overline{I}$, $\overline{II}$, III, $\overline{IV}$, dot search
				⋮	⋮	⋮	⋮	⋮
				1	1	1	1	I, II, III, IV, dot search
	640 × 200, 1 color	1	0	×	×	×	0	$\overline{I}$, dot search
				×	×	×	1	I, dot search
			1	×	0	×	×	$\overline{III}$, dot search
				×	1	×	×	III, dot search
	640 × 200, 4 colors	1	×	×	0	×	0	$\overline{I}$, $\overline{III}$, dot search
				×	0	×	1	I, $\overline{III}$, dot search
				×	1	×	0	$\overline{I}$, III, dot search
				×	1	×	1	I, III, dot search
	MZ-700	0	0	0	0	0	1	Data, ATB, CG area read

(*): Refer to the display frame of Table-1.

NOTES:

- Read for the non-existing VRAM are not assured.
- The above parameter has to be set up for the MZ-700 mode.

★ B/$\overline{A}$ must be set to "0" for the standard MZ-800 (without MZ1R25).

b) Write format register (WR) (OUT & CC)

MSB							LSB
WMD 2	WMD 1	WMD 0	(NOTE) B/$\overline{A}$	IV	III	II	I

NOTE: Same as the bit B/$\overline{A}$ of the read format register.

- I, II, III, IV .....
  Color plane designation

- WMD 0 ~ 2 .....
  Selects the logical operational mode for read-modify-write.

- B/$\overline{A}$ (NOTE)
  Standard MZ-800 → "0": Frame A access .....
  Frame A is accessed for the display mode.
  "1": Frame B access .....
  Frame B is accessed for the display mode.

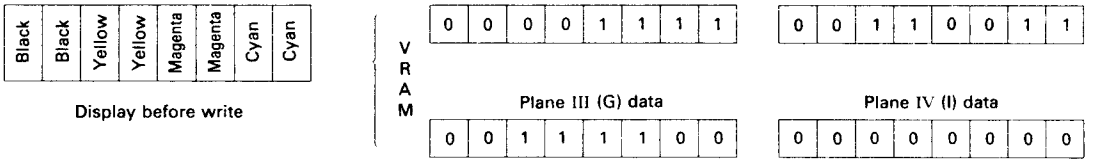
Write mode	WMD 2	1	0	B/$\overline{A}$	Color plane IV	III	II	I	Display mode	Function [WD: Write data, VD: VRAM data]
SINGLE WRITE	0	0	0	(*)	0/1	0/1	0/1	0/1	320 × 200, 4/16 colors 640 × 200, 1/4 colors	Color plane of "1": WD, write Color plane of "0": Fixed
EXOR	0	0	1	Frame A: 0	0/1	0/1	0/1	0/1		Color plane of "1": WD ⊕ VD Color plane of "0": Fixed
OR	0	1	0	Frame B: 1	0/1	0/1	0/1	0/1		Color plane of "1": WD + VD Color plane of "0": Fixed
RESET	0	1	1		0/1	0/1	0/1	0/1		Color plane of "1": $\overline{WD}$ · VD Color plane of "0": Fixed
REPLACE	1	0	×	0	×	×	0/1	0/1	320 × 200 Ⓐ, 4 colors Ⓑ	Writes WD in a specific color (Character write to the graphic plane)
				1	0/1	0/1	×	×		
				×	0/1	0/1	0/1	0/1	320 × 200, 16 colors	Color plane of "1": WD
				0	×	×	×	0/1	640 × 200 Ⓐ, 1 color Ⓑ	Color plane of "0": Writes "0". Color plane of "X": Fixed
				1	×	0/1	×	×		
				×	×	0/1	×	0/1	640 × 200, 4 colors	
PSET	1	1	×	0	×	×	0/1	0/1	320 × 200 Ⓐ, 4 colors Ⓑ	Writes only bit "1" of WD in a specific color. (Character write to graphic plane)
				1	0/1	0/1	×	×		
				×	0/1	0/1	0/1	0/1	320 × 200, 16 colors	Color plane of "1": WD + VD
				0	×	×	×	0/1	640 × 200 Ⓐ, 1 color, Ⓑ	Color plane of "0": $\overline{WD}$ · VD Color plane of "X": Fixed
				1	×	0/1	×	×		
				×	×	0/1	×	0/1	640 × 200, 4 colors	
MZ-700	0	0	0	0	0	0	0	1	MZ-700	Writes WD into the DATA, ATB, and CG area.

(*) Refer to Table-1 display frame

NOTES:
- Write for the non-existing VRAM are not assured.
- The above parameter has to be set up for the MZ-700 mode.
- B/$\overline{A}$ must be set to "0" for the standard version MZ-800.

c) Example of CPU read/write access

- Shown next are access examples of REPLACE write, PSET write, and SEARCH read in the 320 × 200, 16-color mode.
  As for display colors, Plane I corresponds to B, II to R, III to G, and IV to I.

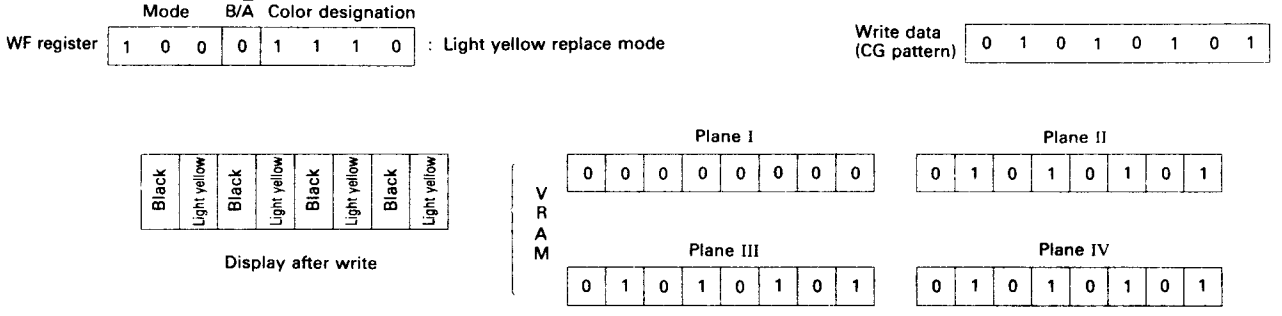


① REPLACE write

- To develop light yellow characters on the graphic screen.

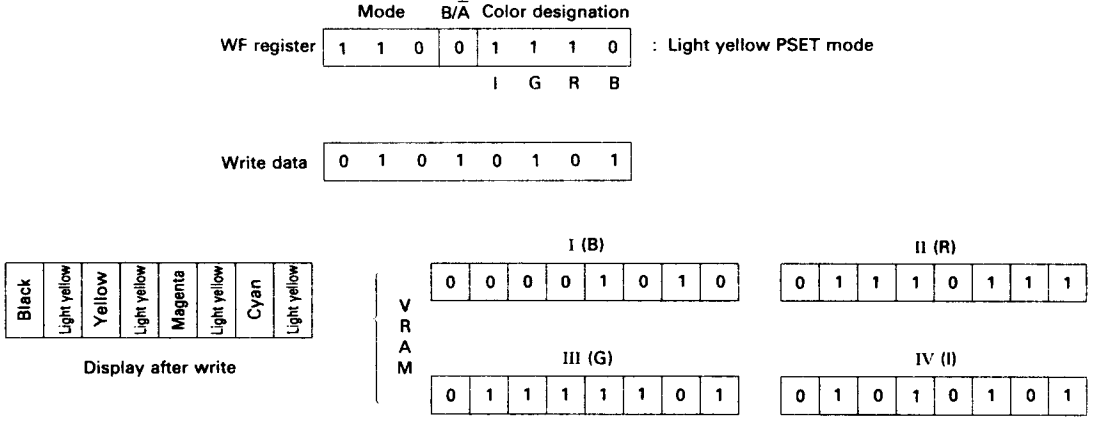
It develops the screen when a next CG patterns are written after setting the REPLACE mode and the light yellow color in the WF register.

So, the bit "1" of the write data becomes the color specified by WF and rest of others become RESET (black).



② PSET write

- To overlay a light yellow hatching over the graphic display screen of ①.

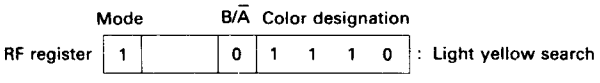


So, only the bit "1" of the write data becomes the color specified by WF in this mode, and rest of other colors do not change.

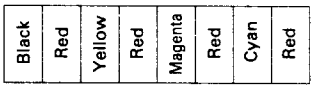
Read data 0 1 0 1 0 1 0 1 : Only the bit of light yellow becomes "1".

③ SEARCH read + PSET write

- To change light yellow in ② above to change to red
- The following data are set when the memory is read after setting the light yellow search mode in the RF register.



- When the above read data are read after setting the red PSET mode in the WR register.

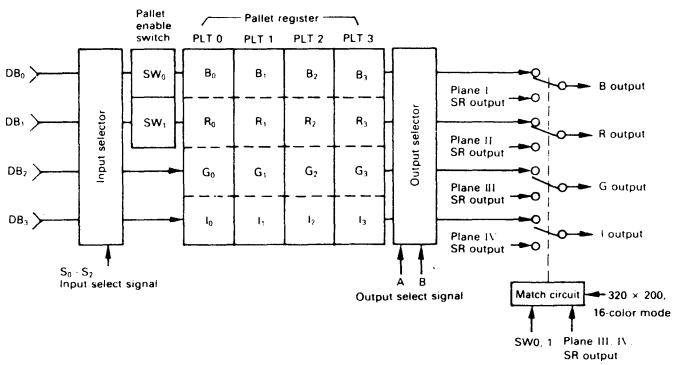


Now, a partial color change has been attained.
As in above, it enhances fast display change with less of VRAM accessing by using various write modes.

4-2-8. Pallet

- As there are four 4-bit pallet registers provided inside the unit, it permits choice of R, G, B, and I combinations, and it enables to make choice of any desired two or four colors out of sixteen available colors. However, in the 320 × 200, 16-color mode, choice of colors permitted to four kinds of colors output of sixteen.
- Only the conventional mode is applicable for the MZ-700 mode without using pallet.
- Pallet is not applicable for the border color.

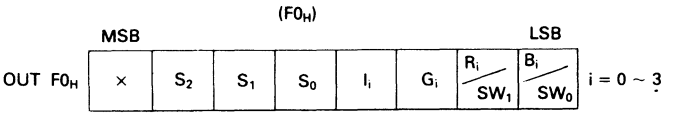
<Configuration>



<Pallet output and display mode>

- Shown next is the relation of the display mode, color plane data vs R, G, G, I outputs.

<Pallet register write> ($F0_H$)



1) $S_0 \sim S_2$: Register section

S_2	S_1	S_0	Register No.
0	0	0	PLT 0
0	0	1	PLT 1
0	1	0	PLT 2
0	1	1	PLT 3
1	0	0	SW_0, SW_1

2) Bi, Ri, Gi, Ii: Pallet write data

3) SW_0, SW_1:
With these switches, it is possible to make combination of Planes III and IV data in the 320 × 200, 16-color mode. Switches are used to assign pallets to four groups of colors.

(Plane III data) = SW_0, (Plane IV data) = SW_1

Only for the color information, the color information set by the pallet register are available as B, R, G, and I outputs. For color information other than that, data in Plane I through Plane IV are sent out as the B, R, G, and I outputs.
(See example next.)

Display mode			Display color	Pallet output select A	Pallet output select B	Pallet enable SW_0, SW_1	Output select A	Output select B	Output	Output	Output	Output
320 × 200	4 color	Frame A	4 colors out of 16 colors	Plane I data	Plane II data	×	0	0	B_0	R_0	G_0	I_0
							1	0	B_1	R_1	G_1	I_1
							0	1	B_2	R_2	G_2	I_2
							1	1	B_3	R_3	G_3	I_3
		Frame B	4 colors out of 16 colors	Plane III data	Plane IV data	×	0	0	B_0	R_0	G_0	I_0
							1	0	B_1	R_1	G_1	I_1
							0	1	B_2	R_2	G_2	I_2
							1	1	B_3	R_3	G_3	I_3
	16 colors	—	(Ex.) 16 colors out of 16 colors	Plane I data	Plane II data	SW_0 = (Plane III data) SW_1 = (Plane IV data)	0	0	B_0	R_0	G_0	I_0
							1	0	B_1	R_1	G_1	I_1
							0	1	B_2	R_2	G_2	I_2
							1	1	B_3	R_3	G_3	I_3
							×	×	I	II	III	IV
640 × 200	2 colors	Frame A	2 colors out of 16 colors	Plane I data	×	×	0	×	B_0	R_0	G_0	I_0
							1	×	B_1	R_1	G_1	I_1
		Frame B	2 colors out of 16 colors	Plane III data	×	×	0	×	B_0	R_0	G_0	I_0
							1	×	B_1	R_1	G_1	I_1
	4 colors	—	4 colors out of 16 colors	Plane I data	Plane III data	×	0	0	B_0	R_0	G_0	I_0
							1	0	B_1	R_1	G_1	I_1
							0	1	B_2	R_2	G_2	I_2
							1	1	B_3	R_3	G_3	I_3

(Ex.)
An example of the pallet in use in the 320 × 200, 16-color mode

- Assume that the pallet register has been set to the following.
  - PLT0 = Black
  - PLT1 = Cyan
  - PLT2 = Red
  - PLT3 = Magenta
- When SW_0 is set to "0" and SW_1 to "0", the pallet is applied to four colors in group 1 (III = 0, IV = 0) and it results in the color as shown in ① of the table right (yellow to cyan).
- When SW_0 is set to "0" and SW_1 to "1", four colors of group 3 (III = 0, IV = 1) becomes the display color set by the pallet.
- Therefore, any color can be chosen out of 16 colors against four colors of color group selected by SW1 and SW2.
- For group other than selected by SW_0 and SW_1, the color that I ~ IV outputted on B, R, G, I is displayed.

Group	Plane data I	II	III	IV	Display color of I ~ IV → RGBI	SW_0 = 0 SW_1 = 0	SW_0 = 0 SW_1 = 1
Group 1	0	0	0	0	Black	**PLT0 = Black**	Black
	1	0	0	0	Blue	**PLT1 = Cyan**	
	0	1	0	0	Red	**PLT2 = Red**	
	1	1	0	0	Magenta	**PLT3 = Magenta**	
Group 2	0	0	1	0	Green	←	←
	1	0	1	0	Cyan	←	←
	0	1	1	0	Yellow	←	←
	1	1	1	0	White	←	←
Group 3	0	0	0	1	Gray	←	**PLT0 = Gray**
	1	0	0	1	Light blue	←	**PLT1 = Light blue**
	0	1	0	1	Light red	←	**PLT2 = Light red**
	1	1	0	1	Light magenta	←	**PLT3 = Light magenta**
Group 4	0	0	1	1	Light green	←	←
	1	0	1	1	Light cyan	←	←
	0	1	1	1	Light yellow	←	←
	1	1	1	1	Light white	←	←

Border color

- As the CRTC has a 4-bit border color register, it permit to use any border color out of 16 colors.
- Border register (OUT $06CF_H$)

	MSB							LSB
BCOL	×	×	×	×	I	G	R	B

- B, R, G, and I becomes "0" (black) when reset.

4-2-9. CRTC register map

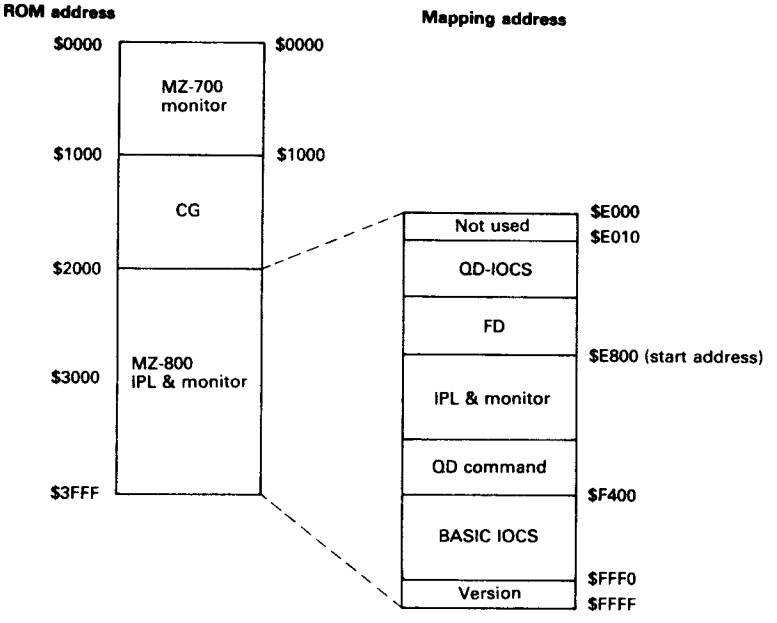
- VRAM control
- Data display on the video screen

Control I/O address map

I/O address H (B)	I/O address L (C, ☆)	IN/OUT		
——	CC	O	Write format register (WF)	
——	CD	O	Read format register (RF)	
——	CE	O	Display mode register (DMD)	
——	CE	I	Status read	
01	CF	O	Scroll offset register L (SOF1), 8 bits	Written by indirect OUT command. B register ← 0~7 OUT(C),A
02	CF	O	Scroll offset register R (SOF2), 2 bits	
03	CF	O	Scroll width register (SW), 7 bits	
04	CF	O	Scroll start address register (SSA), 7 bits	
05	CF	O	Scroll end address register (SEA), 7 bits	
06	CF	O	Border color register (BCOL), 4 bits	
07	CF	O	Superimpose bit (D7) (CKSW), 1 bit	
	FD	O	Pallet register	

4-2-10. ROM configuration

The MZ-700 monitor, character generator (CG), MZ-800 monitor, and IPL are implemented on a single chip of 16k × 8-bit ROM.

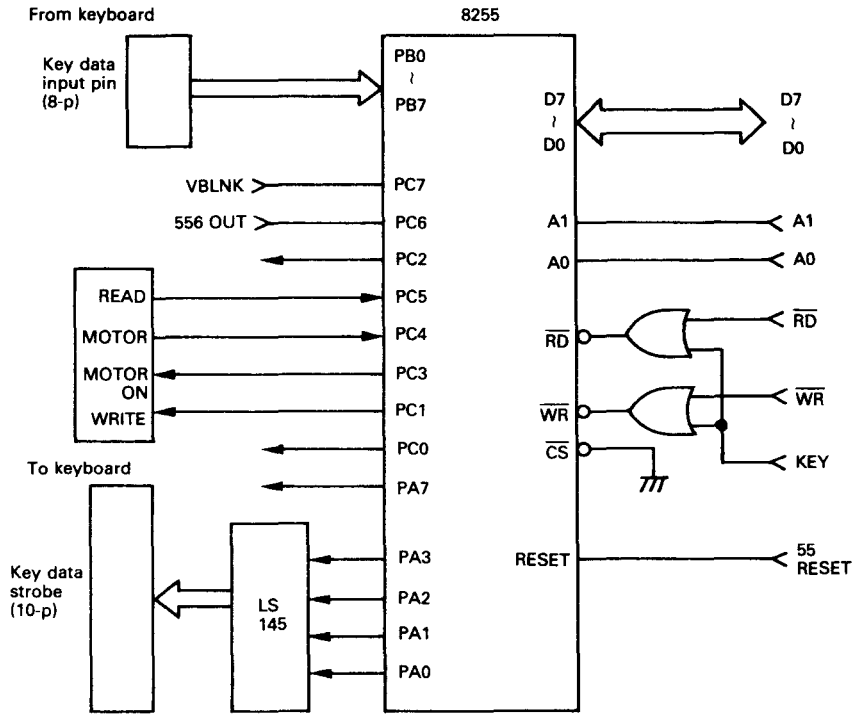


4-3. 8255 Programmable Peripheral Interface

The 8255 has three pairs of 8-bit I/O ports, each one can be assigned to input or output port by means of programming. A different mapping is established depending on the mode. In the MZ-700 mode, it is on memory space, and in the MZ-800 mode, it is on I/O space.

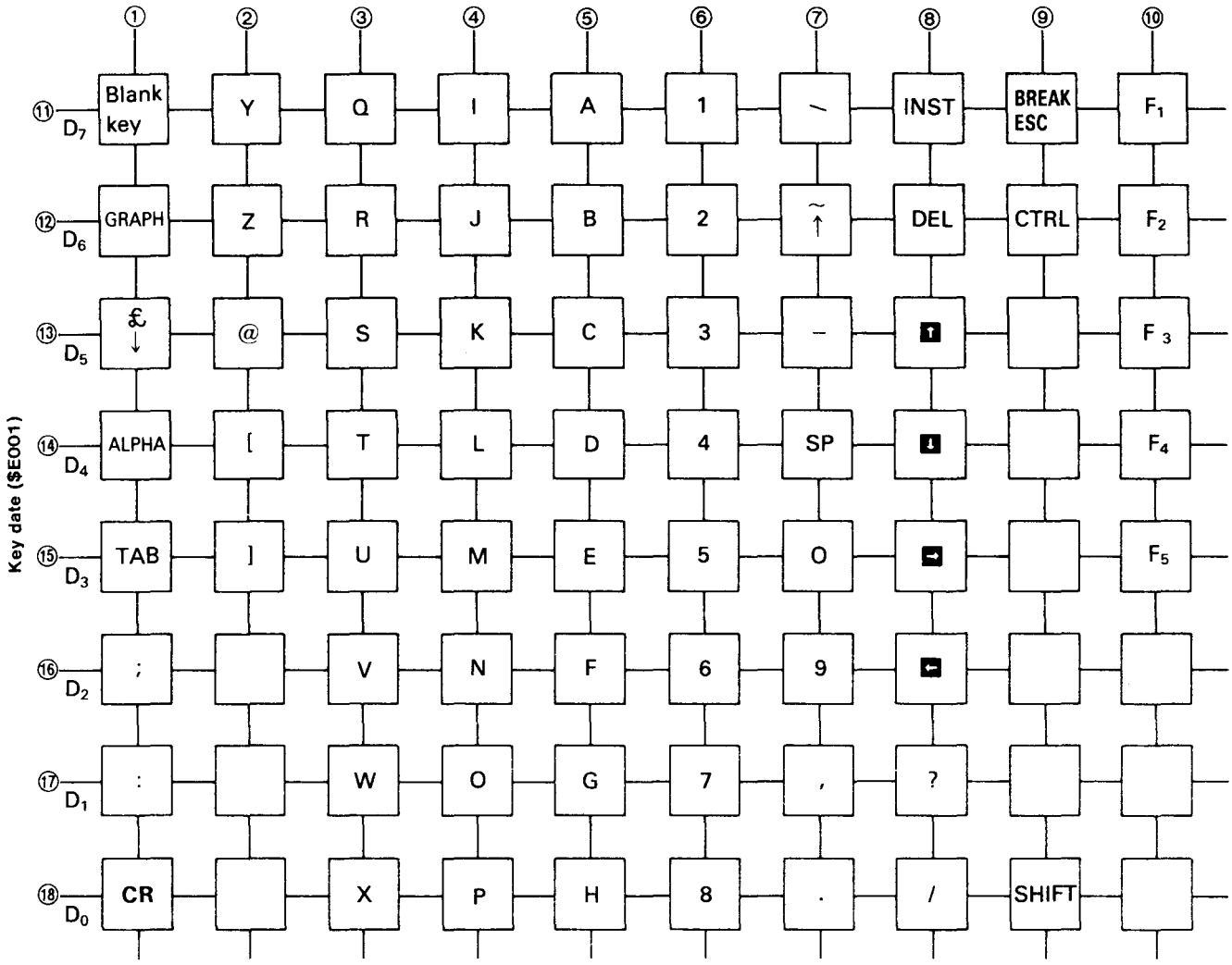
Port name (address)	Pin No.	I/O	Active state	Function
PA (700 $E000 / 800 $D0)	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_7	O	H H H H L L L	Keyboard scan strobe Joystick-1 strobe Joystick-2 strobe CRT cursor blink timer reset
PB (700 $E001 / 800 $D1)	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	I	L L	Keyboard scan input
PC (NOTE-1) (700 $E002 / 800 $D2)	PC_0 PC_1 PC_2 PC_3 PC_4 PC_5 PC_6 PC_7	O O O O I I I I	L —— L (NOTE-2) H —— —— ——	Prohibits sound output of the 8253 Cassette write data Disables timer interrupt Rotates the cassette motor Checks the cassette motor Cassette read data CRT cursor blink timer input Vertical blink signal
(700 $E003 / 800 $D3)	——	——	——	Control port

NOTE-1: Output data dependent on the bit set mode.
NOTE-2: Motor is controlled on and off by the rising edge of the signal.



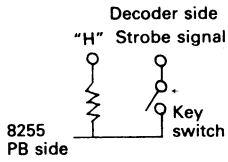
a) Key scan

Ports PA_0~PA_3 of the 8255 are connected via the LS145 decoder, and PB_0~PB_7 are connected to the key matrix directly.



Key strobe is issued through PA_0~PA_3 to scan the key. As it is supplied to the decoder, it makes one of outputs, 0~9, set low. It is then added to the key matrix to scan the line of the key depressed (vertical key matrix scan). The line is in the low state, if it is in depression (horizontal key matrix scan).

NOTE: In the ready for command state, PA_0~PA_3 are normally repeats to be low state and the decoder outputs repeats to be high state. But, since the decoder is of an open collector type, it would not permit to check high and low state.



Example

8255 output PA_3 PA_2 PA_1 PA_0
L H L L

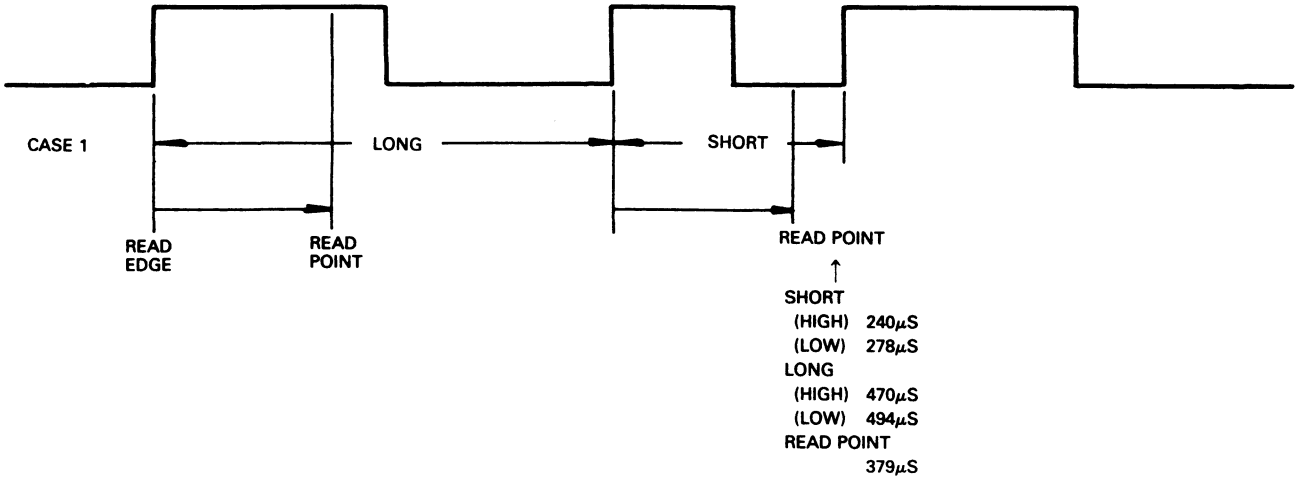
Only the LS145 decoder output 4 (#5 pin) is in low state.

Because the connector (5) is in low state, key scan is permitted only for keys, A through H.

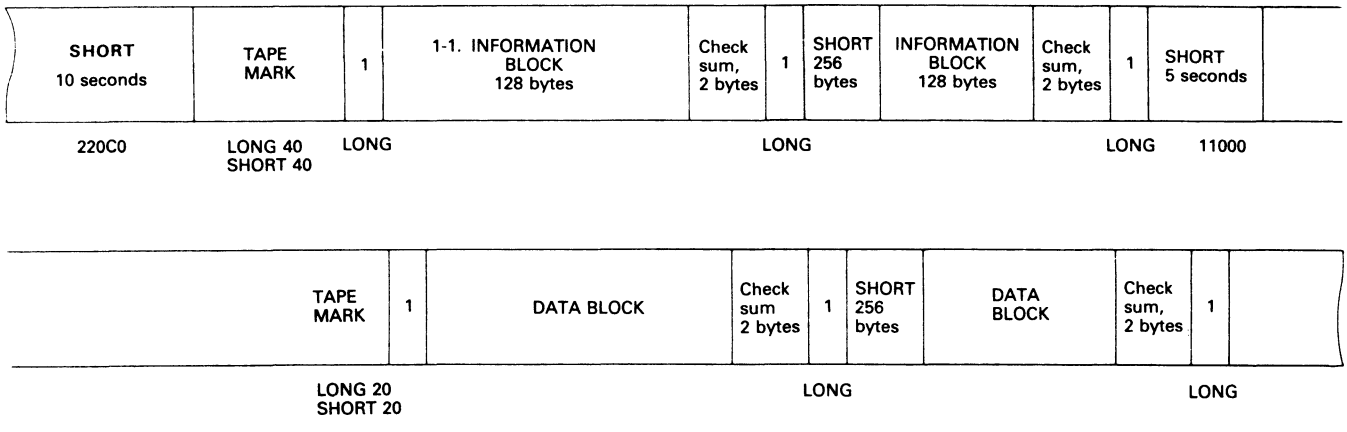
State of the 8255 input port B.
PB_7 PB_6 PB_5 PB_4 PB_3 PB_2 PB_1 PB_0
L H H H L H H L
Above state shows that keys, A, E, or H, is in depression.

b) Cassette control

The 8255 issues the cassette write data from PC1 and read signal through PC5. The type of data (input, output) and its format are as follows:



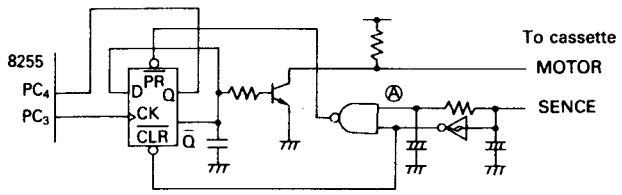
LONG represents the bit value "1" and SHORT the bit value "0". Data will be read at 368 microseconds after the signal rising edge. Data are recorded in repetition of LONG and SHORT, and the same data are written twice.



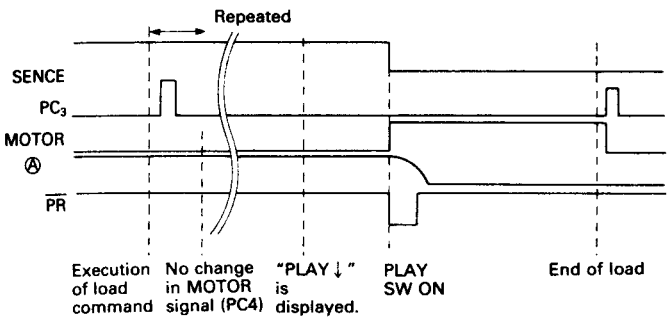
See next for the contents of the information block.

Name	Byte count	Function	Note
ATRB	1	Attribute	
NAME	17	File name (16 characters maximum)	CR (0D) affixed
SIZE	2	File byte size	In order of low to high order
DTADR	2	Loading address	
EXADR	2	Execution address	
COMNT	104	Comment	Not used

Rotation of the cassette (dedicated) is controlled by the 8255 and its peripheral circuits.



If switch has not been ON on the cassette recorder side, SENCE signal is in high state. When a switch (REW, FF, etc.) is pushed, it makes the signal turned low. It presets the D-FF and the motor starts to rotate with MOTOR in high state. With lock given to the D-FF through PC3, it permits on/off control of the motor. If a switch is pushed on the cassette recorder side, it permits examination of the motor operating state by means of L and PC4.

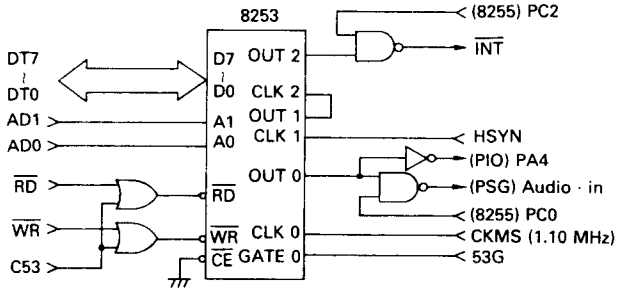


For use of other than MZ-800 cassette tape recorder type, it needs to short SENCE to GND, READ to EXREAD, and WRITE to EXWRITE of the connector T-5. Use of the cassette recorder of other kind may sometimes not permit proper loading and saving operation. In such an event, adjust the volume and tone controls to find the optimum positions. To meet the opposite polarity of cassette tape recorder, there is a dip switch provided. Changing the switch position makes TPSW signal state changed so as to invert the signal waveform.

4-4. 8253 Programmable Interval Timer

The 8253 makes sound generated with the counter #0 and internal timer is operated with the counters #1 and #2.

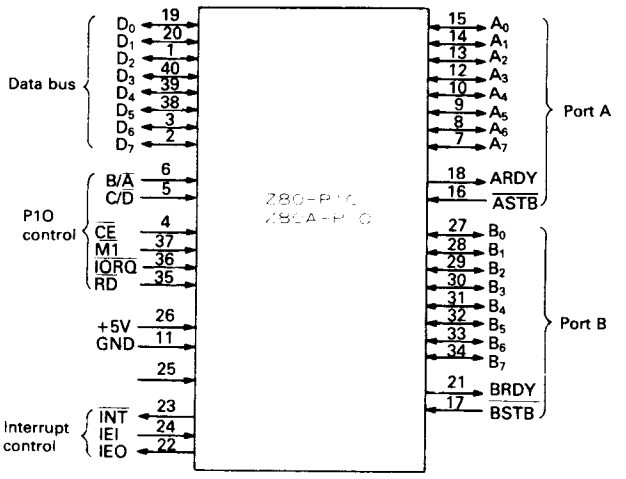
- Counter mode
  #0 ..... Square waveform generator MODE3
  #1 ..... Rate generator MODE2
  #2 ..... Interrupt on terminal counter



- The counter #0 counts input pulse of 1.1 MHz, divided by the predetermined rate (musical score data) to generate sound. It is connected with the mixing audio amplifier through AUDIO-IN of the sound IC (76489AN).
  This counter output is gated by PC of the 8255 port C, and the counter gate is controlled by D01 of $E008. The counter #0 output is also used for interrupt control INT0 and connected to A4 of the Z-80A PIO port A.
- The counter #1 counts pulse of 15.6 kHz and generated a pulse on OUT1 at every second. The counter #2 counts pulses and makes OUT2 turned high. OUT2 outputs becomes $\overline{INT}$ via the gate and is connected to INT of the CPU.

4-5. Printer interface

The Z-80A PIO is used for the printer interface. It has a pair of 8-bit I/O ports.



Pin configuration

<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Signal name</th><th>Description</th></tr>
<tr><td>D_0~D_7</td><td>19,20,1
40,39,38
3,2</td><td>I/O</td><td>Z80-CPU Data Bus</td><td>Bidirectional, 3-state, Z-80 CPU bus.
Data and command transfer between the Z-80 CPU and the PIO is carried out through this data bus. D_0 is the least significant digit.</td></tr>
<tr><td>B/$\overline{A}$</td><td>6</td><td>I</td><td>Port B or A Select</td><td>Port select signal.
Depending on the state of this signal, the port is specified through which data or command is transferred between the Z-80 CPU and the PIO.
H : Port B
L : Port A</td></tr>
<tr><td>C/$\overline{D}$</td><td>5</td><td>I</td><td>Control or Date Select</td><td>Control/data select signal.
Depending on the state of this signal, control port or data port is selected for the port assigned with B/$\overline{A}$.
<table><tr><th>B/$\overline{A}$</th><th>C/$\overline{D}$</th><th>Selected port</th></tr><tr><td>L</td><td>L</td><td>Port A data</td></tr><tr><td>L</td><td>H</td><td>Port A control</td></tr><tr><td>H</td><td>L</td><td>Port B data</td></tr><tr><td>H</td><td>H</td><td>Port B control</td></tr></table></td></tr>
<tr><td>$\overline{CE}$</td><td>4</td><td>I</td><td>Chip Enable</td><td>Chip enable signal.
A low on this line enables the PIO. Normally connected with the I/O address decoder output.</td></tr>
<tr><td>ø</td><td>25</td><td>I</td><td>System Clock</td><td>System clock
CPU clock ø is usually used.</td></tr>
<tr><td>$\overline{M1}$</td><td>37</td><td>I</td><td>Machine Cycle One</td><td>Connection with CPU $\overline{M1}$ signal (low active).
The PIO attains synchronization with the CPU interrupt control logic by $\overline{M1}$. The PIO will be reset when $\overline{M1}$ is set low at least for a period of two clock cycles after turning $\overline{IORQ}$ and $\overline{RD}$ high state.</td></tr>
<tr><td>$\overline{IORQ}$</td><td>36</td><td>I</td><td>Input Output Request</td><td>Connection with CPU $\overline{IORQ}$ signal (low active).
This signal perform data transfer between the CPU and the PIO in connection with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$. If $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are low, the data on the port selected by B/$\overline{A}$ are transferred to the CPU. If $\overline{CE}$, $\overline{IORQ}$ are low, data or command is written through the port selected by B/$\overline{A}$.</td></tr>
<tr><td>$\overline{RD}$</td><td>35</td><td>I</td><td>Read</td><td>Connection with CPU $\overline{RD}$ signal (low active).
This signal controls the direction of data transfer between the CPU and the PIO in connection with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$.</td></tr>
<tr><td>IEI</td><td>24</td><td>I</td><td>Interrupt Enable in</td><td>Interrupt daisy chain signal. The PIO will respond to the INTA cycle of the CPU only when this signal is high.</td></tr>
<tr><td>IEO</td><td>22</td><td>O</td><td>Interrupt Enable Out</td><td>Interrupt daisy chain signal. This signal is high only when IEI is not high with the PIO having an interrupt request. It goes low when IEI is low or PIO is having an interrupt request.</td></tr>
</table>

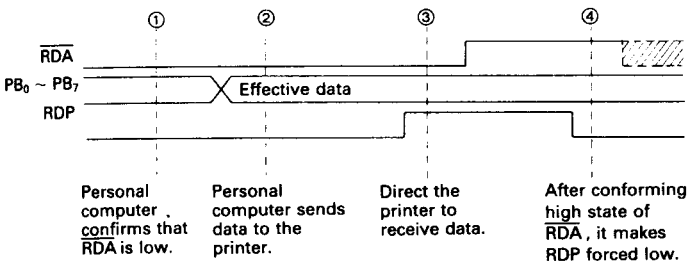
Pin name	Pin No.	I/O	Signal name	Description
$\overline{INT}$	23	O	Interrupt Request	Connection with CPU $\overline{INT}$ signal. A low on this line causes the PIO to place an interrupt request to the CPU. Because it is of an open drain type, it is possible to make $\overline{INT}$ of several peripheral LSI wired OR using the pullup resistance.
A_0~A_7	15–12 10– 7	I/O	Port A Bus	Port A data bus. Data transfer is carried out with the PIO and peripheral device via this bus. A0 is the least significant digit.
$\overline{ASTB}$	16	I	Port A Strobe	Port A strobe. Significance of this signal depends on the Port A operational mode. 1) Byte output mode : It indicates that the peripheral device has received data from the PIO at a riding edge of this strobe. 2) Byte input mode : Peripheral device loads data in the PIO port A input data register at a rising edge of this strobe. 3) Bidirectional mode : The contents of the port A output data register are outputted on A0~A7 when the strobe is in low state. 4) Bit mode : Not used.
ARDY	18	O	Register A Ready	Register A ready. Significance of this signal depends on the state of the port A operational mode. 1) Byte output mode : Data are loaded in the port A data output register when this signal goes high, makes A0~A7 stable, and it indicates that data can be transferred to a peripheral device. 2) Byte input mode : A high on this line indicates that the port A data input register is not occupied so as to be ready for receiving of a next data into the data register. 3) Bidirectional mode : This signal is used to indicate that data has been ready in the port A output data register. Data will not be issued on A0~A7 in this mode, unless $\overline{ASTB}$ turns low. 4) Bit mode : Not used.
B_0~B_7	27–34	I/O	Port B Bus	Port B data bus. Function of this bus is identical to A0~A7. But, it permits to drive a Darlington transistor as the bus can supply 1.5 V, 1.5 mA. B0 is the least significant digit.
$\overline{BSTB}$	17	I	Port B Strobe	Port B strobe. Function of this signal is identical to $\overline{ASTB}$, except for the following: This signal is used to load data from a peripheral device into the port A input data register, when the port A is in the bidirectional mode.
BRDY	21	O	Register B Ready	Register B ready. Function of this signal is identical to ARDY, except for the following: This signal indicates that the port A input data register is unoccupied and is ready for receiving of a next data, when the port A is in the bidirectional mode.

For the MZ-800 the PIO located on the I/O space, and address of ports performs the following:

$FC	Port A control
$FD	Port B control
$FE	Port A data
$FF	Port B data

	Pin name	I/O	Active	Signal name	Function
Port A ($FE)	PA_0	IN	L	$\overline{RDA}$	A low on this line indicates that the printer data is ready to receive.
	PA_1	IN	L	$\overline{STA}$	A low on this line informs the personal a paper depletion during status check.
	PA_2	IN	—	GND	
	PA_3	IN	—	GND	
	PA_4	IN	H		An 8253 output used for interrupt.
	PA_5	IN	H		Horizontal blanking signal used for interrupt.
	PA_6	OUT	H	IRT	Used for printer initialization.
	PA_7	OUT	H	RDP	Indicates the printer to receive data.
Port B ($FF)	PB_0	OUT	—	RD_0	Printer data or control code to the printer.
	PB_1	OUT	—	RD_1	
	PB_2	OUT	—	RD_2	
	PB_3	OUT	—	RD_3	
	PB_4	OUT	—	RD_4	
	PB_5	OUT	—	RD_5	
	PB_6	OUT	—	RD_6	
	PB_7	OUT	—	RD_7	

Interfacing timing



After the personal computer confirms that the printer is ready to receive data at (①), the data is then sent to $FF port (PIO port B) at step (②).
As reception of data is directed to the printer at step (③), it makes RDP forced low at step (④) upon confirming that the printer received it ($\overline{RDA}$=H). After this, it awaits until $\overline{RDA}$ goes from high to low before transfer of a next data. But, it is possible to transfer successive data by interrupting the CPU at a falling edge of $\overline{RDA}$, since RDA is inputted to the $\overline{RSTB}$ input of the PIO, when in the port B mode 0.
It is also possible to interrupt the CPU referring to Port A inputs. Though discussed above is the printer interface method for the MZ compatible printer types, there is the Centronics compatible method for parallel interfacing of the printer. Since this method is basically the same as the MZ mode, except that signal polarity is opposite.

MZ specification		Centronics specification	
Signal name	Active	Signal name	Active
RDA (NOTE)	"L"	BUSY	"H"
RDP	"H"	STB	"L"
IRT	"H"	INPUT PRIME	"L"

NOTE: Though $\overline{RDA}$ is active low, it may be handled the same as high state of BUSY when considered in term of signal significance.

As shown in the figure above, it could be known that RDP and IRT should be inverted in order to make connection with the Centronics compatible printer.
It can be attained by changing PRSW to high using the dip switch.

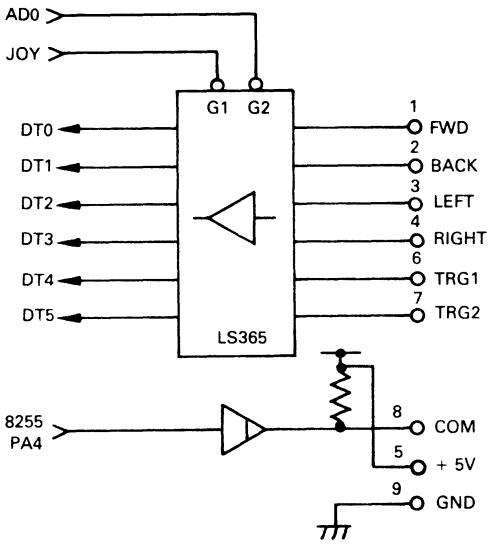
NOTE: When the MZ-800 dedicated printer is used, there may be such a case that proper operation is not attained due to different printing characters and control codes. It must be also noted that all MZ-800 characters can not be printed. Besides, connection with a Centronics compatible printer may not be permitted hardware-wise, sometimes.

4-6. Programmable sound generator

The SN76489N is used for the programmable sound generator which is controlled by the I/O port $F2. It is write only. In order to permit smooth sound generation, timer interrupt is applied using the 8253. For the interrupt timer, the count 0 of the 8253 is used. The counter 0 is used for creation of sound steps in the MZ-700 mode, but, it is used for the timer interrupt source of the PSG in the MZ-800 mode. Interrupt is controlled by PA5 of the PIO. it is, however, possible to mask the counter 0 output by PC0 of the 8255, in order to prevent sound generation during interrupt.

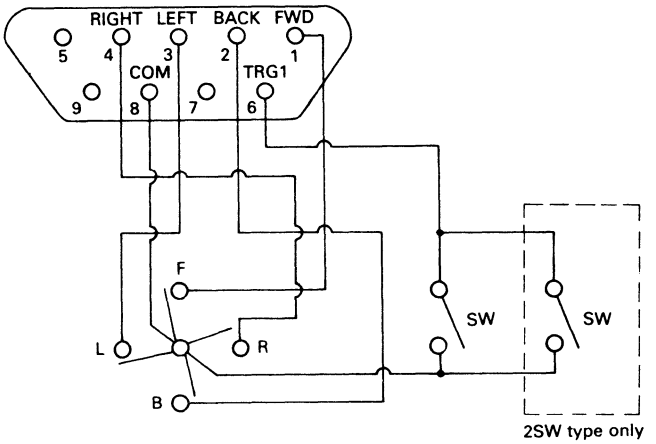
4-7. Joystick

It permits connection of two ATARI compatible joysticks.



(Configuration of joystick-1)

Low active strobes are issued through PA4 (JOY1) of the 8255 and PA5 (JOY2) interrogate switch activation through inputs to $F0 (JOY1) and $F1 (JOY2).



Configuration of ATARI compatible joystick

4-8. System switch setup

System switches are assigned as follows:

SW No.	Function	Setup method
1	MZ-700/MZ-800 selection	ON: MZ-700 mode OFF: MZ-800 mode
2 3	MZ/Centronics printer selection	MZ printer with SW2 and SW3 at ON Centronics printer with SW2 and SW3 at OFF
4	External cassette recorder polarity selection	Changed so as to enable read on the external cassette recorder.

* Switch setups at the factory

SW1 ..... OFF (MZ-800 mode)

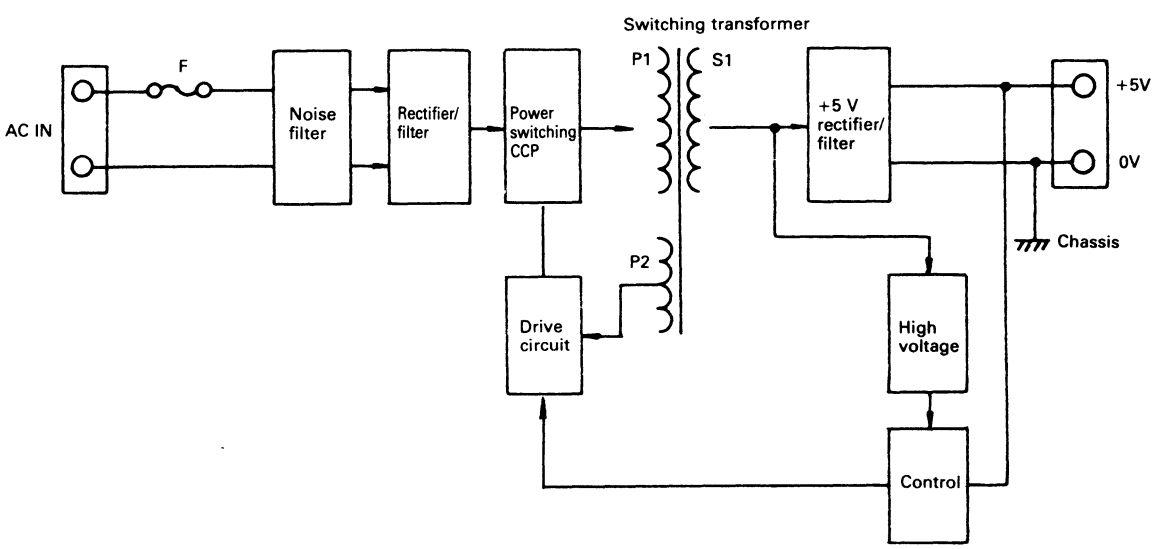
SW2 ..... ON } (MZ dedicated printer)

SW3 ..... ON }

SW4 ..... ON —

5. Power supply

5-1. Block diagram



5-2. Operational description

The block diagram of the power supply unit is shown above. It adopts the self-excitation ON/ON control method. First, the source supply is rectified through the noise filter and converted into direct current. As the dc current is applied to the switching transistor, it causes the transistor to start repeating ON and OFF. After the dc voltage is converted into high frequency pulse, it is added to the primary side of the main transformer which causes to induce voltage on the secondary side. This high frequency pulse is then rectified and filtered to obtain the dc voltage of +5 volts. For control of output voltage, the output voltage is compared with the reference voltage and its error is detected in the control section. While the switching transistor is in the OFF cycle, it makes the photo cuppler PC1 active by the detecting signal of the control section for given period. By adjusting control current of the drive circuit, it makes the out put stabilized.

5-3. Maintenance

Cleaning

Dust deposit inside the power supply unit may becomes the cause for overheat as it prevent heat dispersion, which results in damage in component. Stains on the fuse contact and connector contact may lead to contact failure. So, it has to be cleaned using soft cloth dampened with alcohol or dry soft cloth.

5-4. Problem determination and sequence

Follow the next procedure to find the cause of trouble.

(1) Avoid removing the board to check. But visually observe the board to check for open circuit line, burnt resistor, fuse, and semiconductor chips in the first place.

(2) If a defective item were found, it has to be replaced with the new one. But, care must also taken as there are possible defects in multiple number of components.

≪MZ1P16≫

1. SPECIFICATION

Outline

The MZ-1P16 is the external installation 4-color plot printer designed for use with the MZ-800 series personal computer. It can be fixed on the MZ-800 when the table is used.

Specification

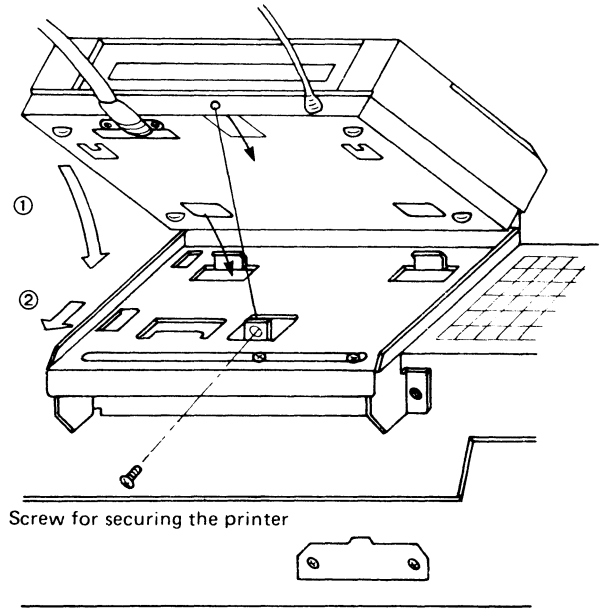
Type name	:	MZ1P16
Print method	:	1, Black; 2, Blue; 3, Green; 4, Red
Print speed	:	10 characters average (smallest letter)
Printing size	:	80/40/26 digits (software assigned)
Character set	:	115
Resolution	:	0.2 mm
Power supply	:	+5 V supplied from the MZ-800 via the DC jack
Power consumption	:	11 W
Physical dimensions	:	162(W) × 133(D) × 59(H), excluding accessories.
Weight	:	1 kg (MZ-1P16)
Accessories	:	Roll paper (1), ball point pen (one each of black, blue, green, red), paper holder (one each on side), paper shaft (1), paper guide (1)
Operating temperature	:	0 to +35 centigrades
Storage temperature	:	−20 to +70 centigrades
Operating humidity	:	80%RH, maximum

2. INSTALLATION

(Fixing the printer)

1. Fix the printer unit on the table as shown in the figure.
   (Place the printer in the arrow direction ①, lightly move in the arrow direction B, then secure it with screws.)

* It is also possible to use the printer free on the table without securing.



Connection procedure after the installation

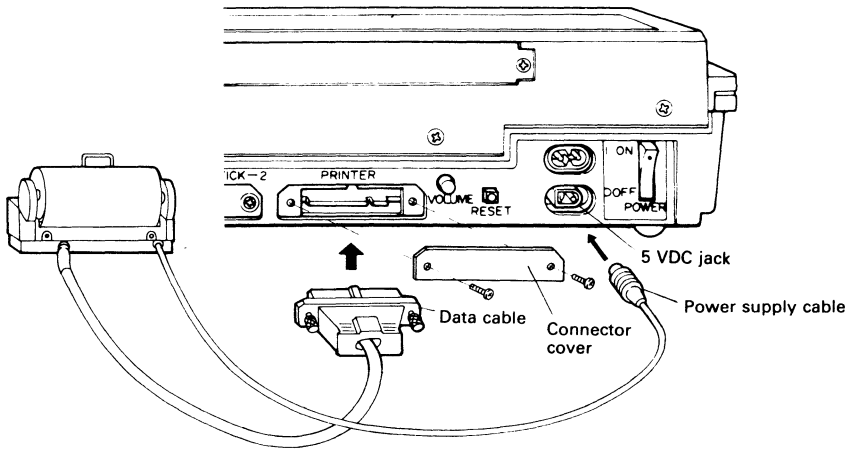
① Make sure that power is off to the MZ-800 and its peripheral units.

② Remove the printer connector cover on the back side of the MZ-800.

③ Connect the data cable and the power supply cable of the unit with the printer connector and the 5 VDC jack of the MZ-800.

④ For connection of the printer connector, use the screws that had been at both ends of connector.

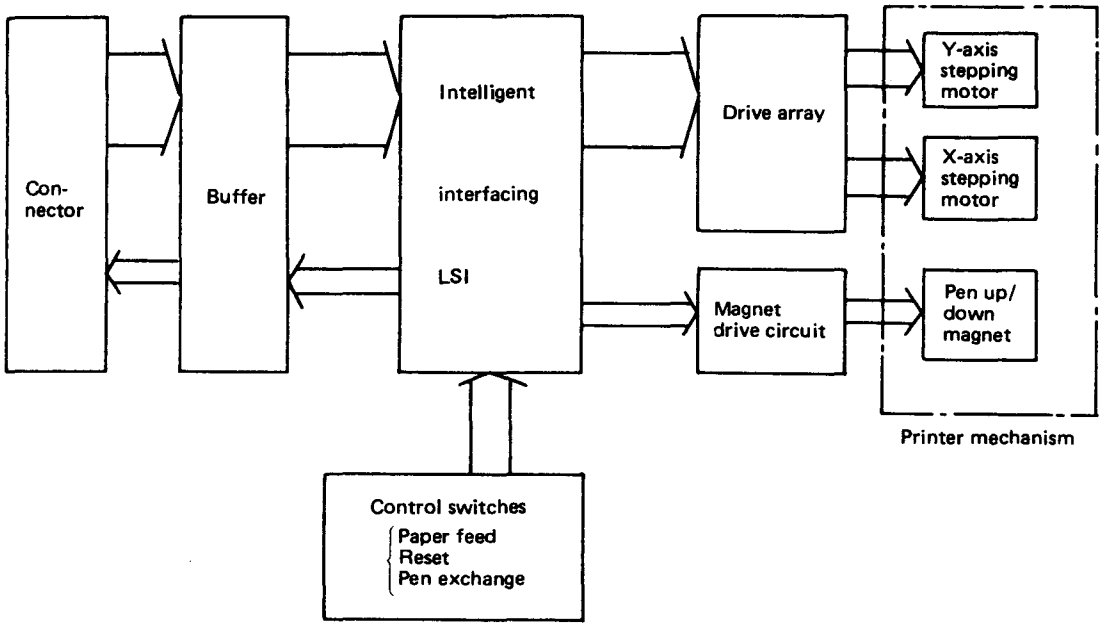
Rear side of the MZ-800



* When this unit is in use, set the MZ-800 printer dip switch to the MZ side.

3. OPERATION

3-1. Block diagram



3-1-1. At power on

At power on, more than 5V of pen up current is applied for a period of 10ms, plus 5 and minus 0ms, to move the carriage 556 steps backward on the X-axis in order to initialize the colour position. As the carriage is held at the left margin after disengagement of the motor, it is then moved 30 steps forward on the X-axis, then stepped back 30 steps again to check if the colour position detector has been made. If not, it continues to move the carriage 30 steps forward on the X-axis, then return 30 steps to ensure the made condition.

3-1-2. Colour change operation

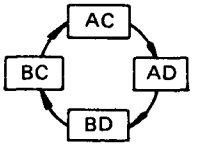
To change colour, the slider makes three reciprocating movements of 6mm (30 steps) at the left end of the X-axis to move the pen position one step. When the desired pen position is attained, it then returns to the home position. Since the pen rotor makes a unidirectional rotation at the left end of the X-axis, and is locked within printable range, care must be exerted not to touch the rotor and the slider.

3-1-3. Pen exchange operation

A pen needs to be exchanged with a fresh one when it runs out of ink. In such an event, the pen is moved 485 steps forward on the X-axis from the home position with the used pen located on the top of the rotor, then take out the used pen, by pressing the pen release lever and exchange it with a fresh one.

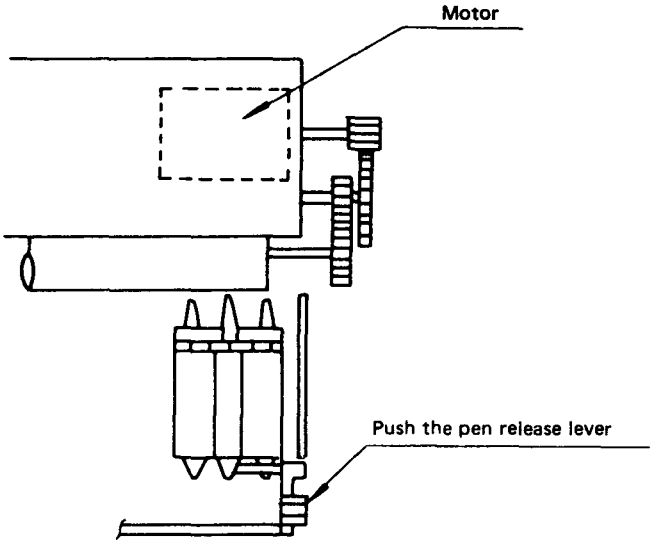
3-1-4. Motor phase and rotating direction

The arrow head indicates the forward direction for both the X-axis and Y-axis.



3-2. Pen exchange method

To remove pen, press the pen exchange button, when the slider is at the right handside, push the pen release lever.

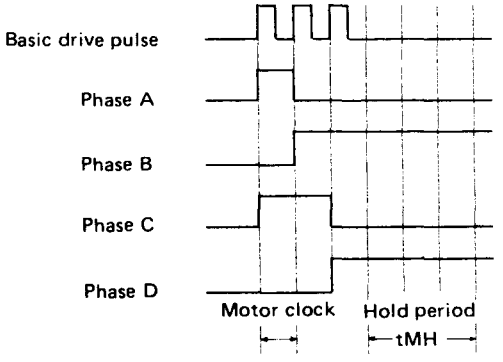


To install the pen, push the tip of the pen through the ring of the return spring in the first place, then push into the holder. Upon completion, ensure that the tip of the pen is engaged with the hole of the pen return spring. If colour change is done when the pen is disengaged from the hole, it may cause improper rotation of the rotary holder as the slider makes contact with the pen. Do not try to rotate the rotary holder by hand when installing the pen during replacement of the pens.

3-3. Stepping motor driving signal

- The X-axis stepping motor and the Y-axis stepping motor are driven by the two-phase magnet.

Stepping motor driving signal



It is more effective to save power to shut off current while the X and Y axis motors are at a halt. But, there may be a possible malfuction because of unsuppressed vibration, if the current is turned off with a normal pulse width. In order to prevent this, current is applied excessively for more than the given hold time (tMH = 1ms or more).

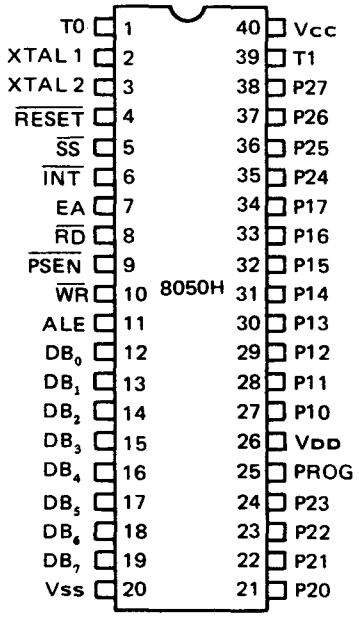
3-4. Colour position detector

The colour position detector consists of a reed switch and a permanent magnet and it may cause malfunction owing to external vibration, and magnetic influence. Especially, when deposit of alien matter or paper fragments is between the left end of the carriage and the frame this may result in a failure of the colour detect performance.

3-5. Character set

Input of an undefined code up to $20 is ignored. Other undefined codes are represented in hexadecimal notation using the pen in a next color position.

Pin configuration (top view)



Pin Configuration

3-6. Colour plotter printer control LSI

Pin assignment

Symbol	Name	In/out	Function
V_{SS}	Ground		Connected to 0V.
V_{CC}	Main power		Connected to 5V.
V_{DD}	Power		Connected to 5V.
PROG	Program	Out	Not used.
$P1_0 \sim P1_7$	Port 1		Used as printer control signals.
$P2_0 \sim P2_7$	Port 2		Used for data input port from CPU.
$D_0 \sim D_7$	Data bus		Used for stepper motor control signals.
T_0	Test pin 0	In	Input from pen change switch.
T_1	Test pin 1	In	Input from paper feed switch.
$\overline{INT}$	Interrupt input	In	Data transfer strobe MZ-700 → MZ1P01.
$\overline{RD}$	Read signal	In	Not used.
$\overline{WR}$	Write signal	Out	Not used.
$\overline{RESET}$	Reset	In	Used to initialize the processor.
ALE	Address latch enable	Out	Not used.
$\overline{PSEN}$	Program store enable	Out	Not used.
$\overline{SS}$	Single step	In	Not used.
EA	External access	In	Active when EA = 0V.
X_1, X_2	Crystal inputs	In	Pins used to attach the crystal oscillator or RC network to generate internal clock. However, external clock signal may be inputted through these pins.

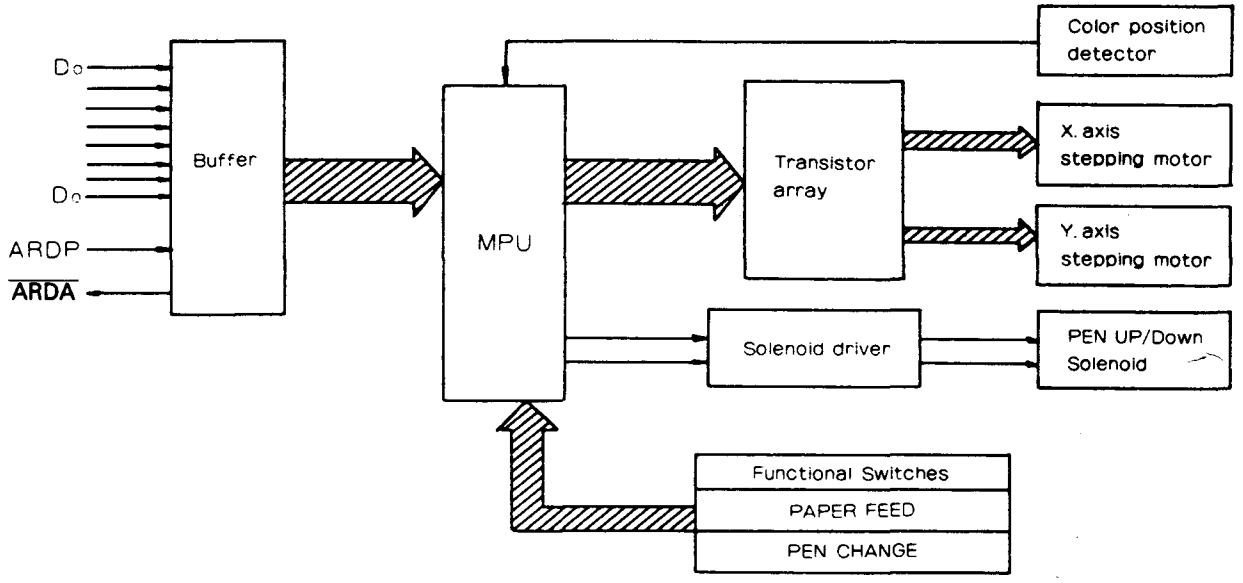
3-7. Interfacing with the MZ-800

Fig. 1 shows the block diagram for connection with the printer. Fig. 2 shows its circuit description. Fig. 3 shows the timing chart.

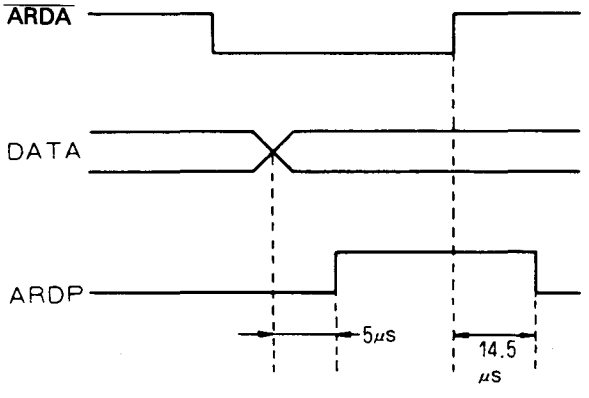
Table of character set

MSD / LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			SP	0	@	P			}		ｱ	ﾝ				
1		↓	!	1	A	Q					ｲ					
2		↑	"	2	B	R				ｪ	ｳ	ﾕ				
3		→	#	3	C	S				ｧ	ｴ	ﾑ				
4		←	$	4	D	T				ｰ	ｵ					
5		HOME	%	5	E	U					ｶ					
6		CLR	&	6	F	V				ｦ	ｷ		→			
7			'	7	G	W				ｱ	ｸ	ｮ		=		
8			(	8	H	X				ｲ	ｹ	ｯ				
9			)	9	I	Y				ｳ	ｺ	ｱ゛				
A			*	:	J	Z				ｴ	ｻ	ｲ゛				
B			+	;	K	[		°	^	ｵ	ｼ	ｳ゛				ｴ゛
C			,	<	L	¥				ｶ						ｵ゛
D			-	=	M	]				ｷ	ｽ	ｶ゛				
E			.	>	N	↑				ｸ	ｾ	ｷ゛				
F			/	?	O	←				ｹ	ｿ		ｰ			ﾟ

3-8. Block diagram



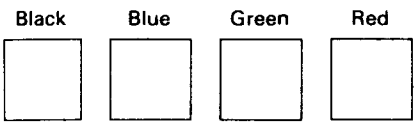
The CPU sends data to the printer after confirming that ARDA is in low state. Five micro seconds later, the strobe signal ARDP goes high. The CPU confirms that ARDA is in high state, ARDP is returned to a low state 14.5 micro seconds later.



4. COLOR PLOTTER-PRINTER CONTROL CODES

4-1. Control codes used in the text mode

- Text code ($01)
  Places the printer in the text mode.
- Graphic code ($02)..... Same as the BASIC PMODE statement.
  Places the printer in the graphics mode.
- Line up ($03)..... Same as the BASIC PSKIP statement.
  Moves the paper one line in the reverse direction. The line counter is decremented by 1.
- Pen test ($04)..... Same as the BASIC PTEST statement.
  Writes the following patterns to start ink flowing from the pens, then sets scale = 1 (40 chr/line), colour = 0.



- Reduction scale ($09) + ($09) + ($09)
  Reduces the scale from 1 to 0 (80 chr/line).
- Reduction cancel ($09) + ($09) + ($0B)
  Enlarges the scale from 0 to 1 (40 chr/line).
- Line counter set ($09) + ($09) + $(ASCII)_2$ + $(ASCII)_1$ + $(ASCII)_0$ + ($0D)
  ..... Same as the BASIC PTEST statement.
  Specifies the number of lines per page as indicated by the 3 ASCII bytes code. The maximum number of lines per page is 255. Automatically set to 66 when the power is turned on or the system is reset.
- Line feed ($0A)..... Same as the BASIC PSKIP statement.
  Moves the paper one line in the forward direction. The line counter is incremented by 1.
- Magnify scale ($0B)
  Enlarges the scale from 2 to 1. (26 chr/line)
- Magnify scale ($0C)
  Reduces the scale from 2 to 1.
- Carriage return ($0D)
  Moves the carriage to the left side of the print area.
- Back space ($0E)
  Moves the carriage one column to the left. This code is ignored when the carriage is at the left side of the print area.
- Form feed ($0F)
  Moves the paper to the beginning of the next page and resets the line counter to 0.
- Next colour ($1D)
  Changes the pen to the next colour.

4-2. Character scale

- The character scale is automatically set to 1 (40 chr/line) when the power is turned on. Afterwards, it can be changed by the control codes and commands.
- In the graphics mode, the scale can be changed within the range 0 to 63.
- The scale is set to 1 when the mode is switched from graphics to text.

4-3. Graphic mode commands

4-3-1. Command type

In the graphics mode, the computer can control the printer with the following commands. The words in parentheses are BASIC statements which have the same functions as the graphics mode commands.

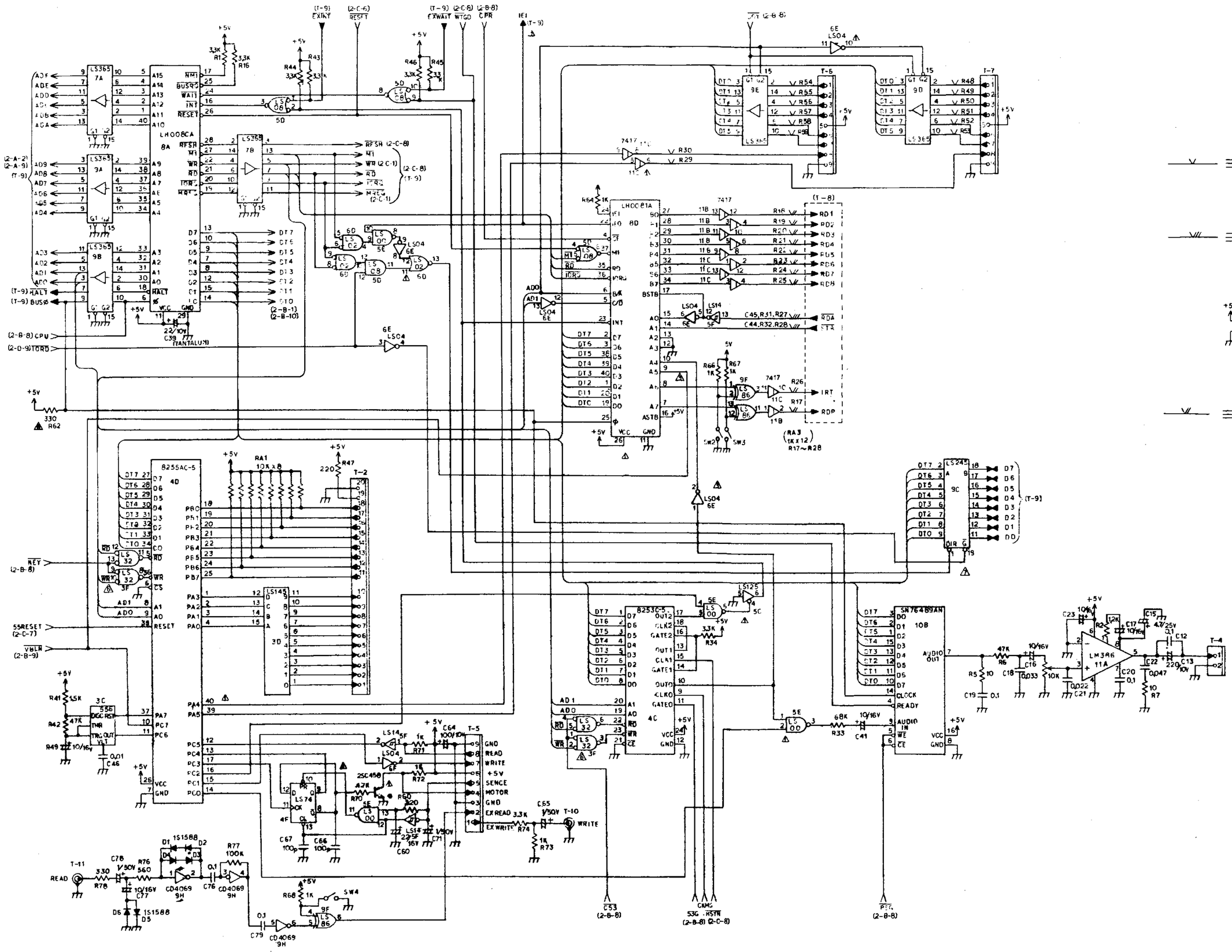
Command name	Format	Function
LINE TYPE	Lp (p=0 to 15)	Specifies the type of line (solid or dotted) and the dot pitch. p=0 : solid line, p=1 to 15 : dotted line
ALL INITIALIZE	A	Places the printer in the text mode.
HOME (PHONE)	H	Lifts the pen and returns it to the origin (home position).
INITIALIZE (HSET)	I	Sets the current pen location as the origin (x=0, y=0).
DRAW (LINE)	Dx, y, ..., xn, yn ($-999 \leqq x, y \leqq 999$)	Draws lines from the current pen location to coordinates (x_1, y_1), then to coordinates (x_2, y_2), and so forth.
RELATIVE DRAW (RLINE)	JΔx, Δy, ..., Δxn, Δyn ($-999 \leqq \Delta x, \Delta y \leqq 999$)	Draws lines from the current pen location to relative coordinates (Δx_1, Δy_1), then to relative coordinates (Δx_2, Δy_2) and so forth.
MOVE (MOVE)	Mx, y ($-999 \leqq x, y \leqq 999$)	Lifts the pen and moves it to coordinates (x, y).
RELATIVE MOVE (RMOVE)	RΔx, Δy ($-999 \leqq \Delta x, \Delta y \leqq 999$)	Lifts the pen and moves it to coordinates (Δx, Δy).
COLOR CHANGE (PCOLOR)	Cn (n=0 to 3)	Changes the pen colour to n.
SCALE SET	Sn (n=0 to 63)	Specifies the character scale.
ALPHA ROTATE	Qn (n= 0 to 3)	Specifies the direction in which characters are printed.
PRINT	$Pc_1c_2c_3$ ... cn (n=∞)	Prints characters.
AXIS (AXIS)	Xp, q, r (p=0 or 1) (q= $-$999 to 999) (r=1 to 255)	Draws an X axis when p=1 and a Y axis when p=0. q specifies the scale pitch and r specifies the number of scale marks to be drawn.

4-3-2. Command format

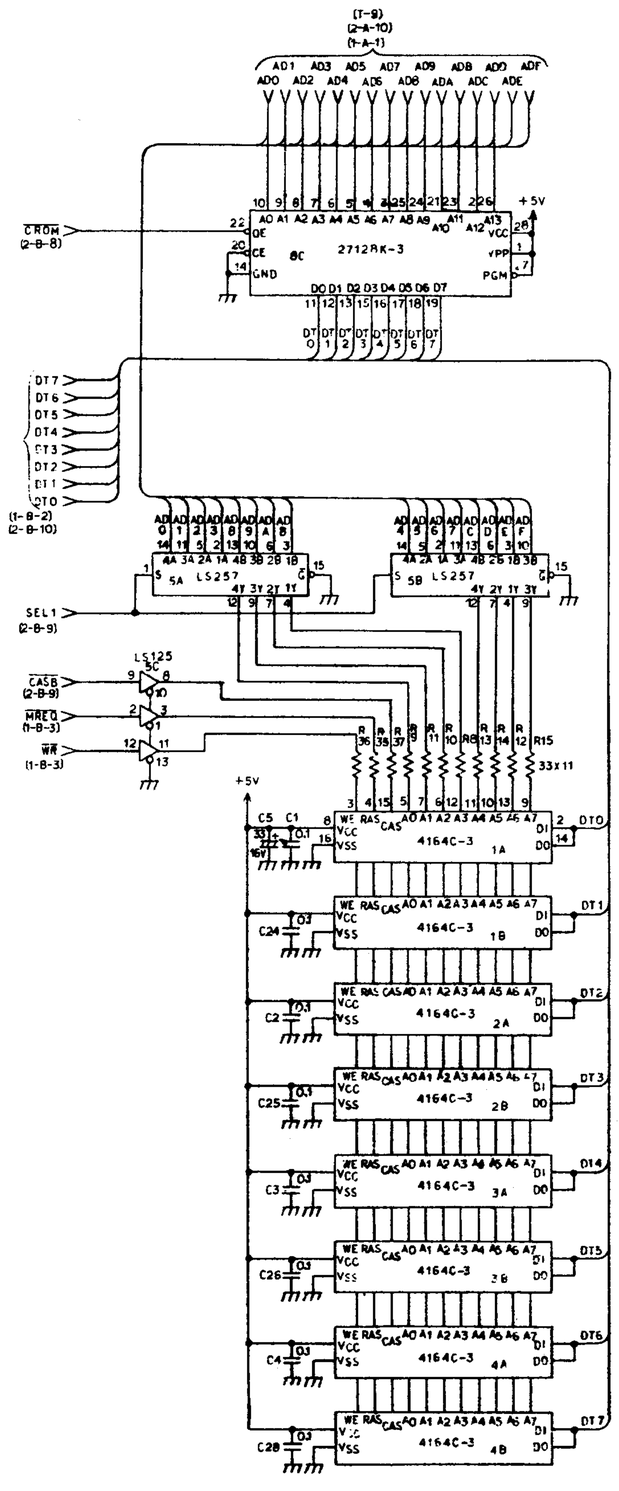
There are 5 types of command formats as shown below.

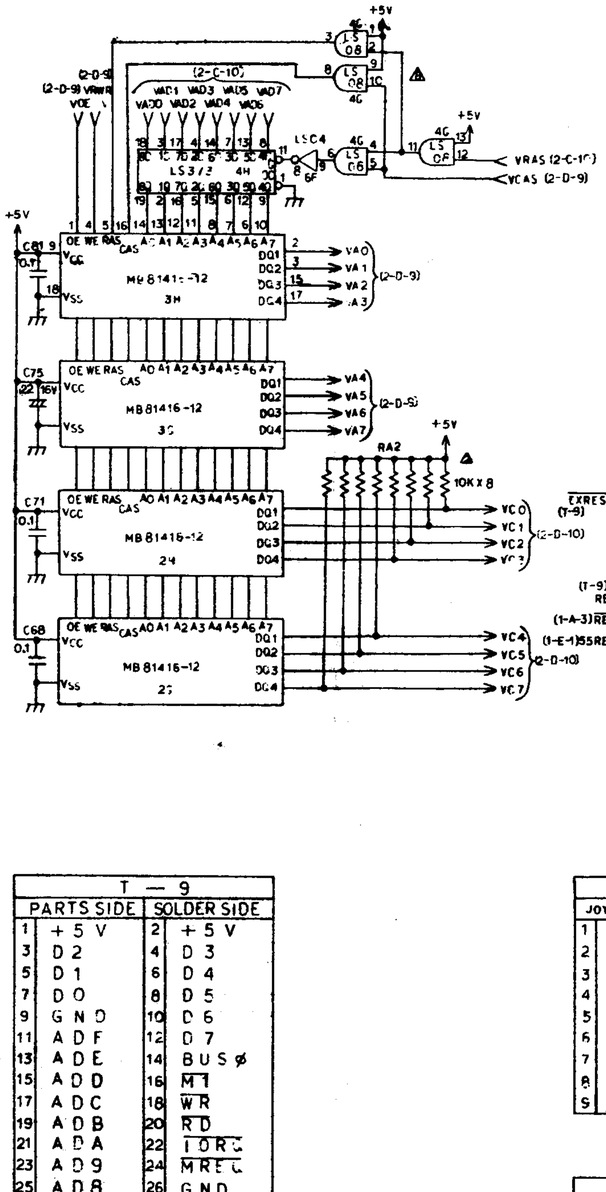
1. Command character only (without parameters)
   A , H , I
2. Command character plus one parameter
   L , C, S , Q
3. Command character plus pairs of parameters
   D , J , M , R
   " , " is used to separater parameters, and a CR code is used to end the parameter list.
4. Command plus character string
   P
   The character string is terminated with a CR code.
5. Command plus three parameters
   X
   " , " is used to separate parameters.

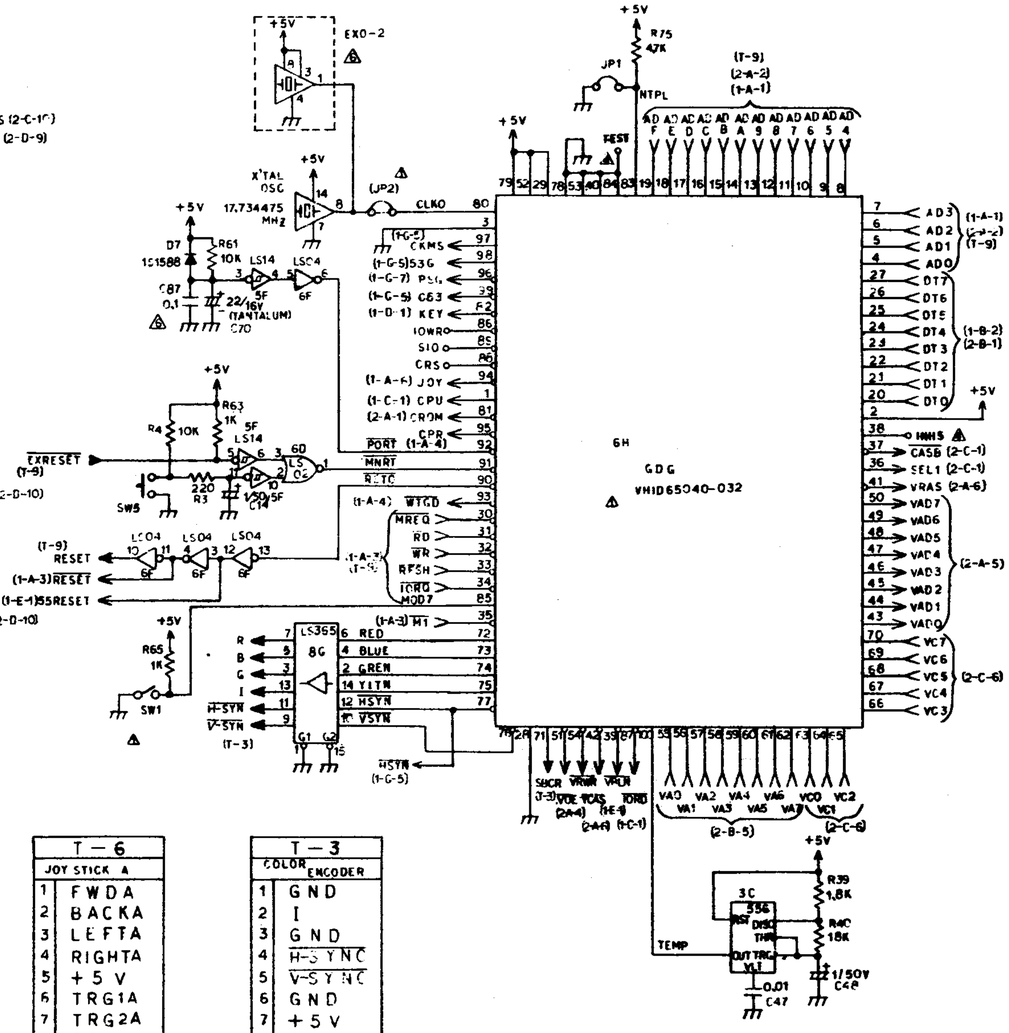
MZ-800 CPU P.W.B. Circuit ½



MZ-800 CPU P.W.B. Circuit 2/2







T — 9			
PARTS SIDE		SOLDER SIDE	
1	+5V	2	+5V
3	D2	4	D3
5	D1	6	D4
7	D0	8	D5
9	GND	10	D6
11	ADF	12	D7
13	ADE	14	BUSØ
15	ADD	16	$\overline{M1}$
17	ADC	18	$\overline{WR}$
19	ADB	20	$\overline{RD}$
21	ADA	22	$\overline{IORC}$
23	AD9	24	$\overline{MREC}$
25	AD8	26	GND
27	AD7	28	$\overline{HALT}$
29	AD6	30	IEI ⚠
31	AD5	32	NC.
33	AD4	34	RESET
35	AD3	36	$\overline{EXRESET}$
37	AD2	38	$\overline{INT}$
39	AD1	40	$\overline{EXWAIT}$
41	AD0	42	NC.
43	GND	44	GND

T — 6	
JOY STICK A	
1	FWDA
2	BACKA
3	LEFTA
4	RIGHTA
5	+5V
6	TRG1A
7	TRG2A
8	COMA
9	GND

T — 7	
JOY STICK B	
1	FWDB
2	BACKB
3	LEFTB
4	RIGHTB
5	+5V
6	TRG1B
7	TRG2B
8	COMB
9	GND
10	GND
11	SW1
12	SW2
13	SW3
14	SW4
15	+5V

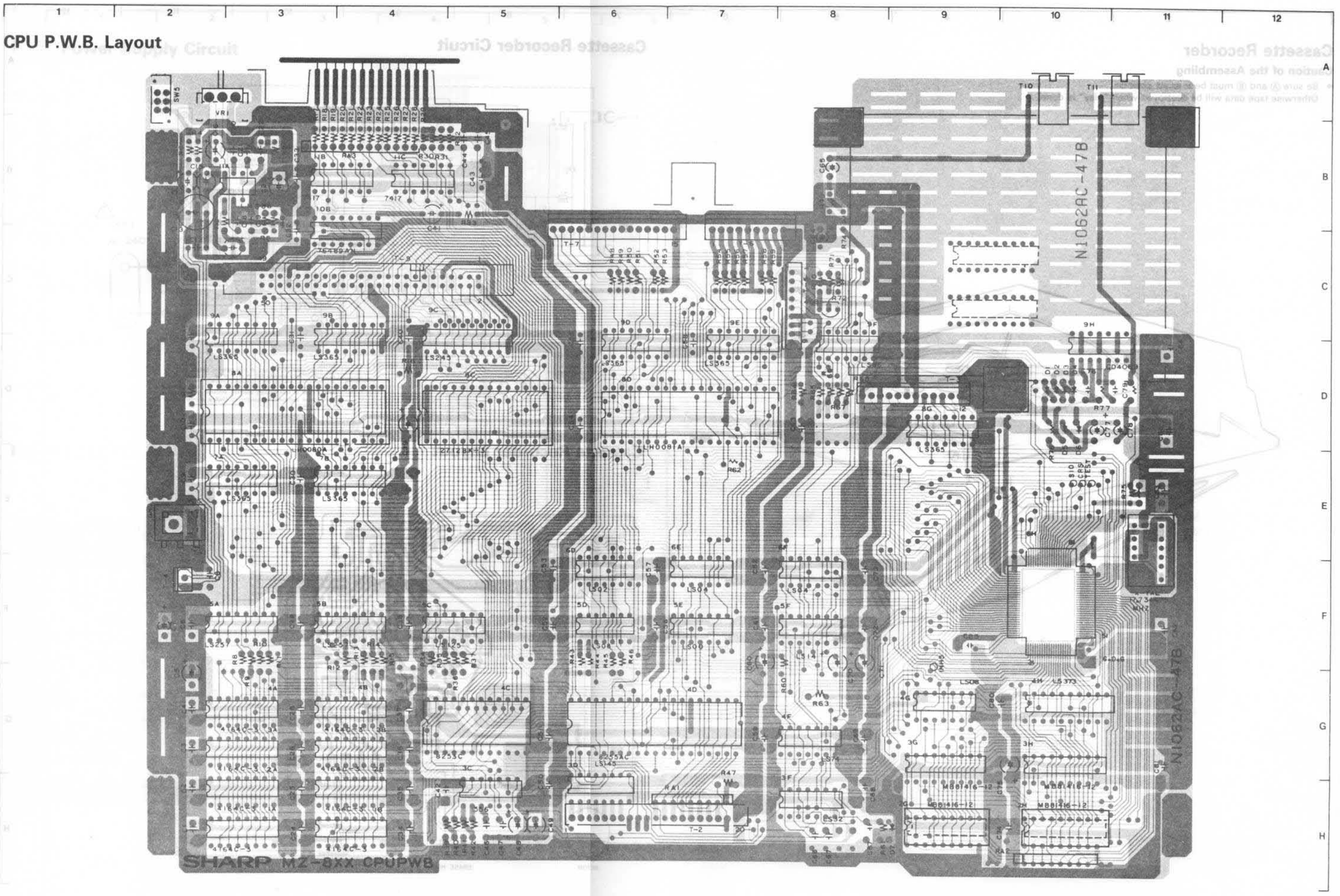
T — 3	
COLOR ENCODER	
1	GND
2	I
3	GND
4	$\overline{H\text{-}SYNC}$
5	$\overline{V\text{-}SYNC}$
6	GND
7	+5V
8	G
9	B
10	R
11	SBCR
12	GND

Din Buchse

1 1
2 ⊥
3 unused
4 H-Sync
5 V-Sync
6 R
7 G
8 B

T — 8			
PARTS SIDE		SOLDER SIDE	
1	RDP	2	GND
3	RD1	4	GND
5	RD2	6	GND
7	RD3	8	GND
9	RD4	10	GND
11	RD5	12	GND
13	RD6	14	GND
15	RD7	16	GND
17	RD8	18	GND
19	IRT	20	GND
21	$\overline{RDA}$	22	GND
23	$\overline{STA}$	24	GND
25	GND	26	GND

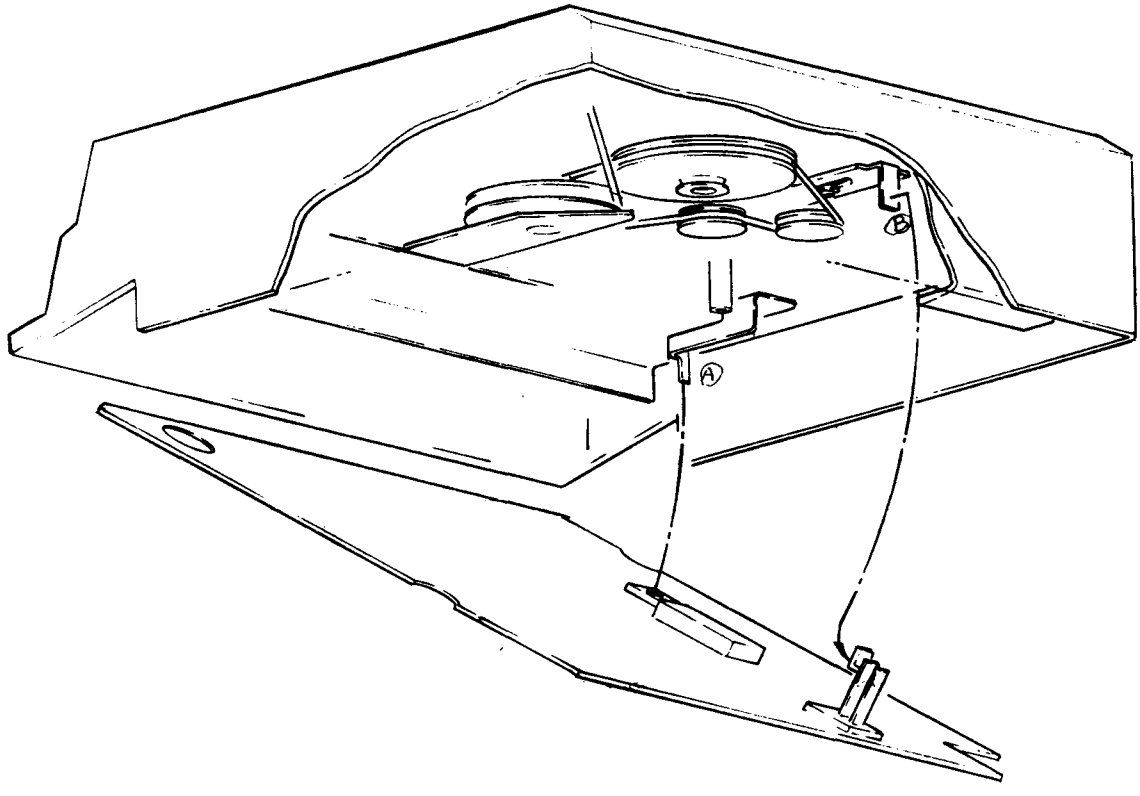
CPU P.W.B. Layout



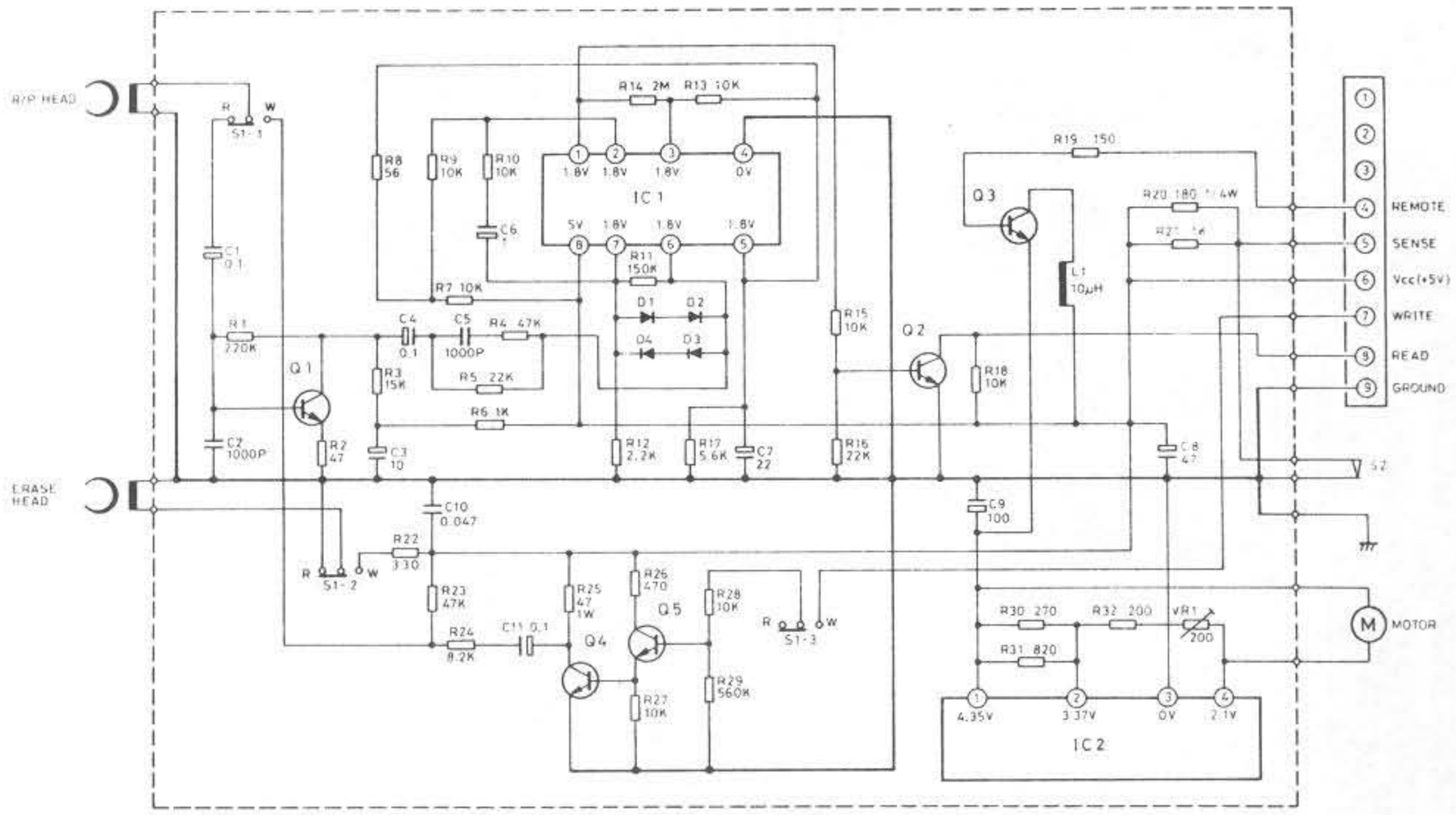
Cassette Recorder

Caution of the Assembling

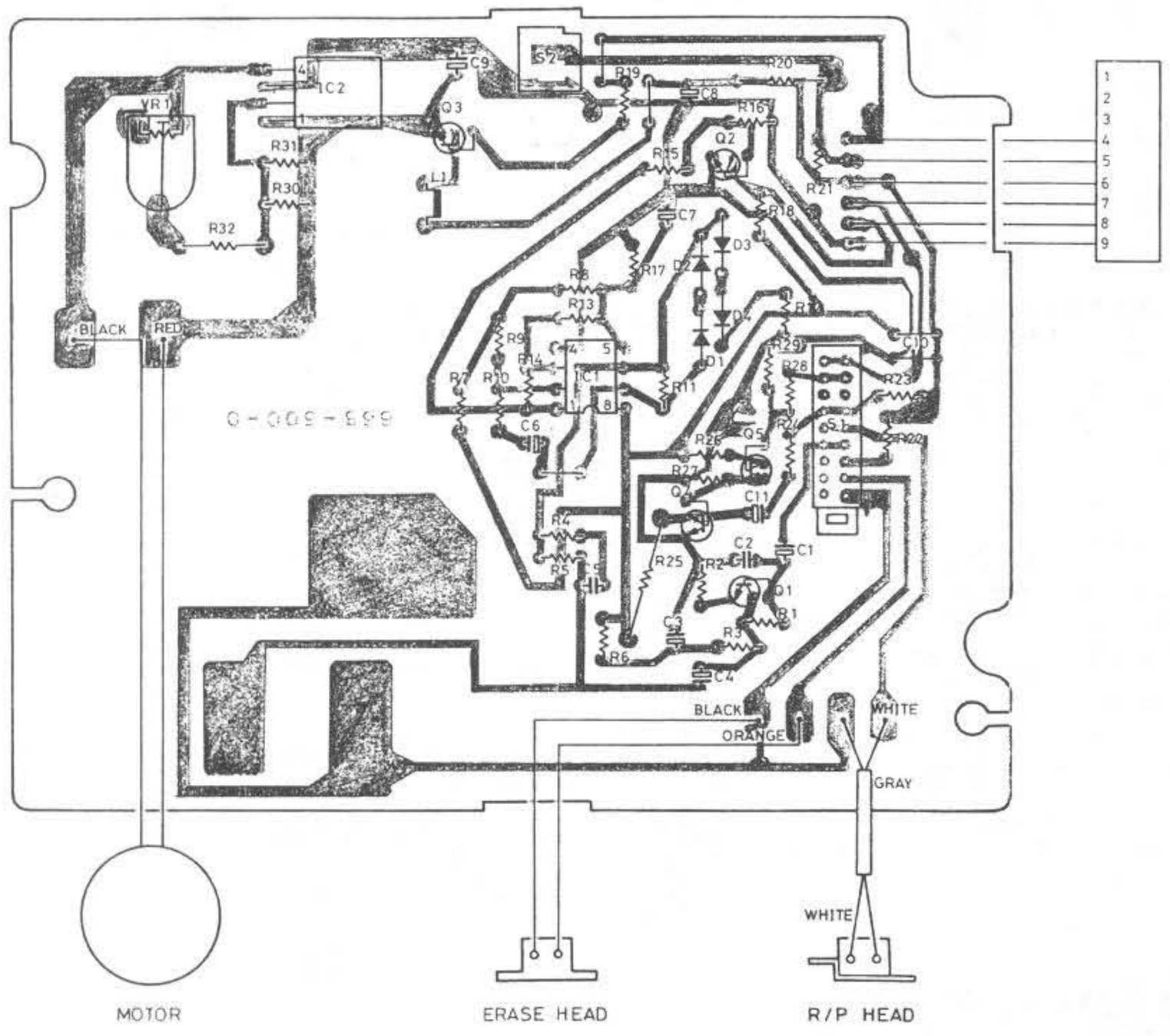
- Be sure Ⓐ and Ⓑ must be in exact position.
  Otherwise tape data will be destroyed when "play" is done.



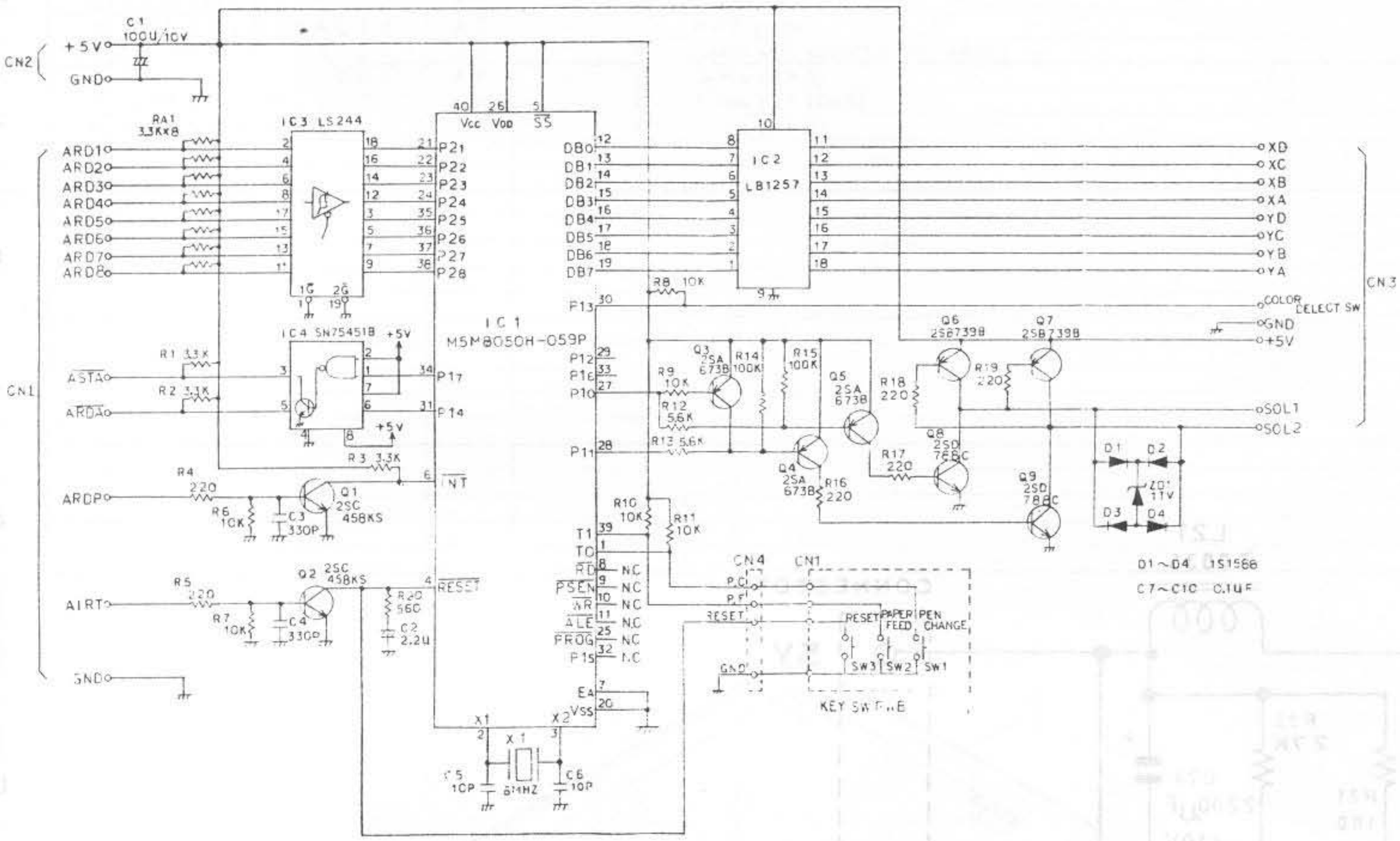
Cassette Recorder Circuit



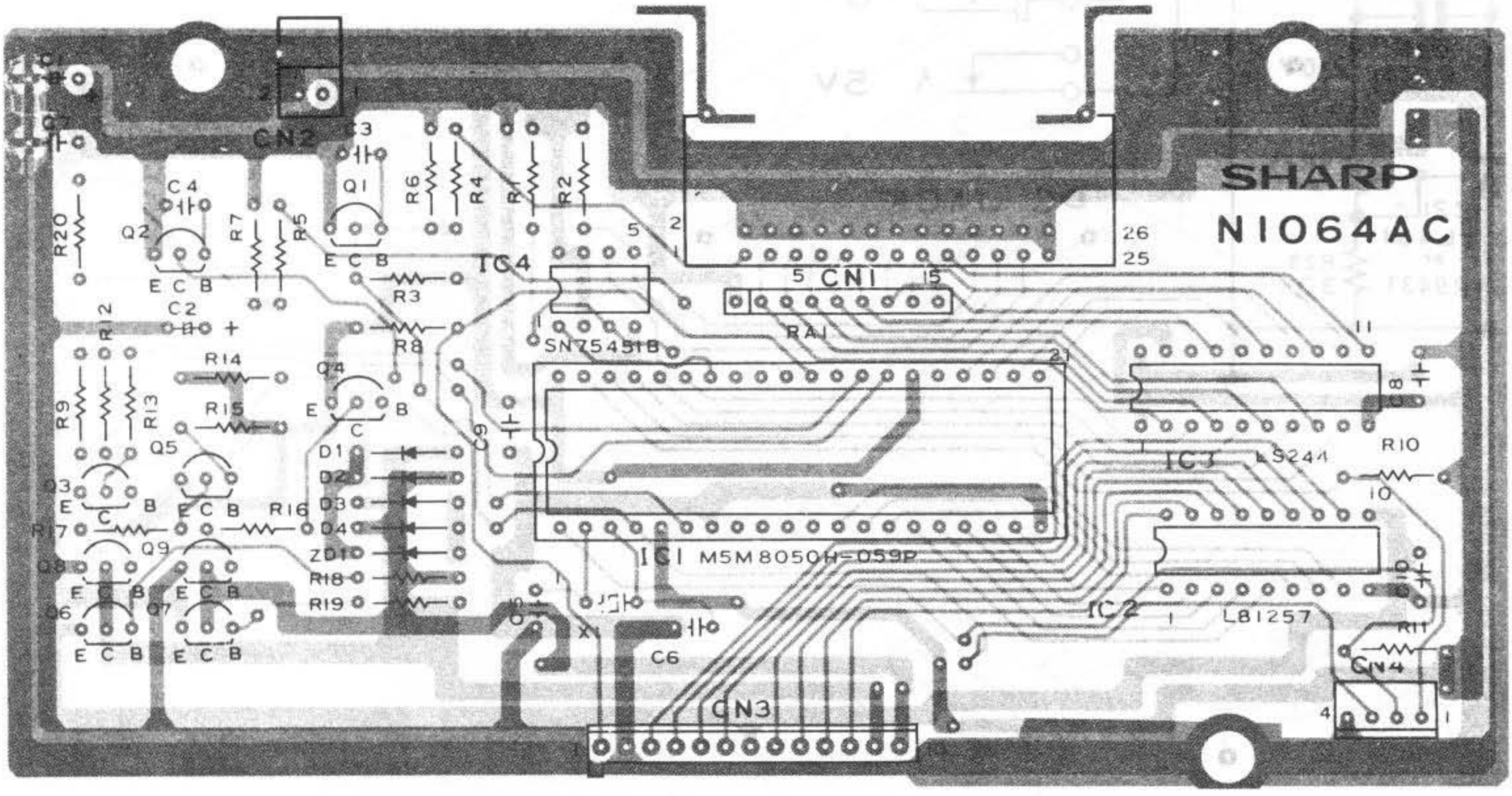
Cassette Recorder Layout



MZ-1P16 CIRCUIT

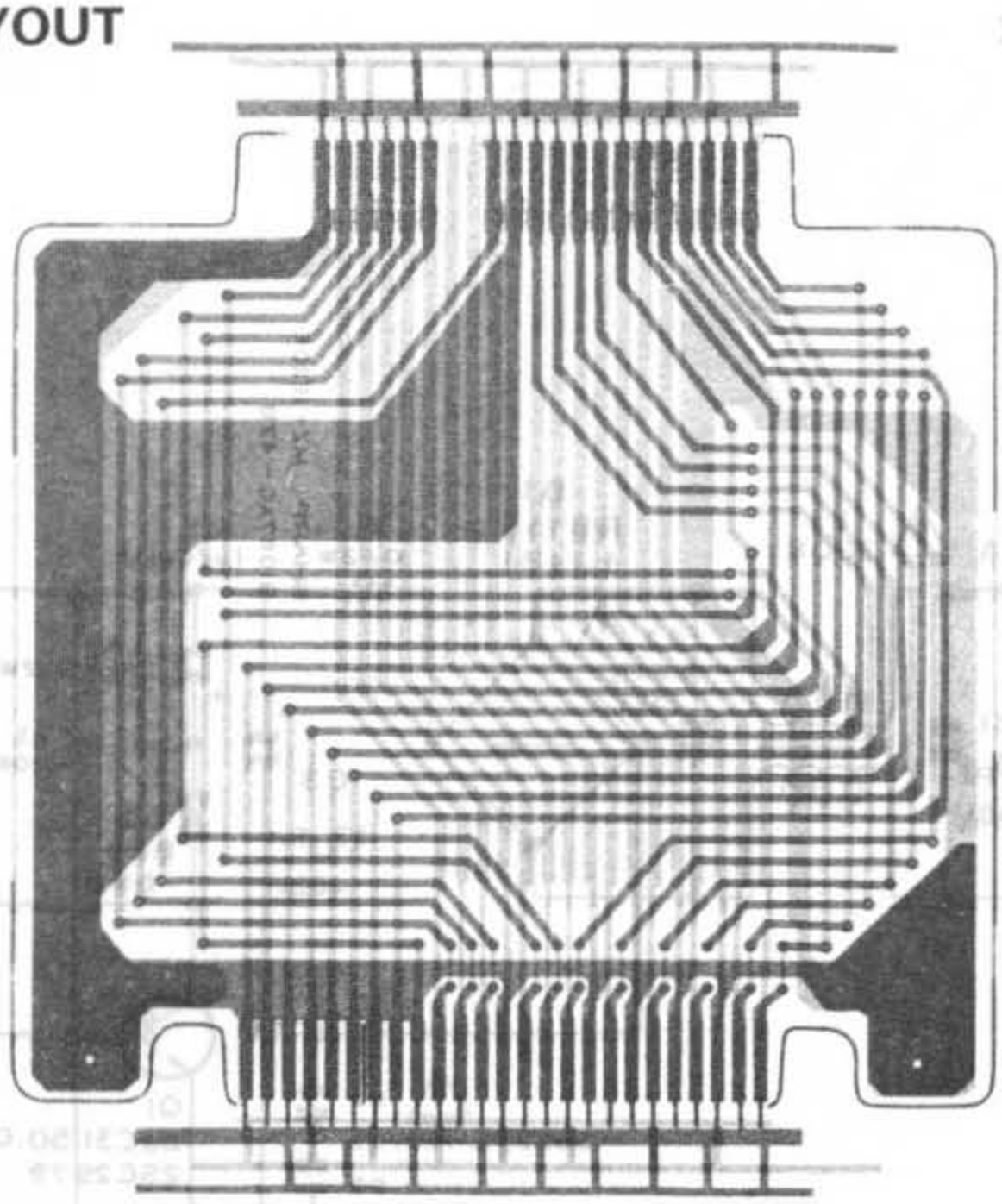


MZ-1P16 LAYOUT



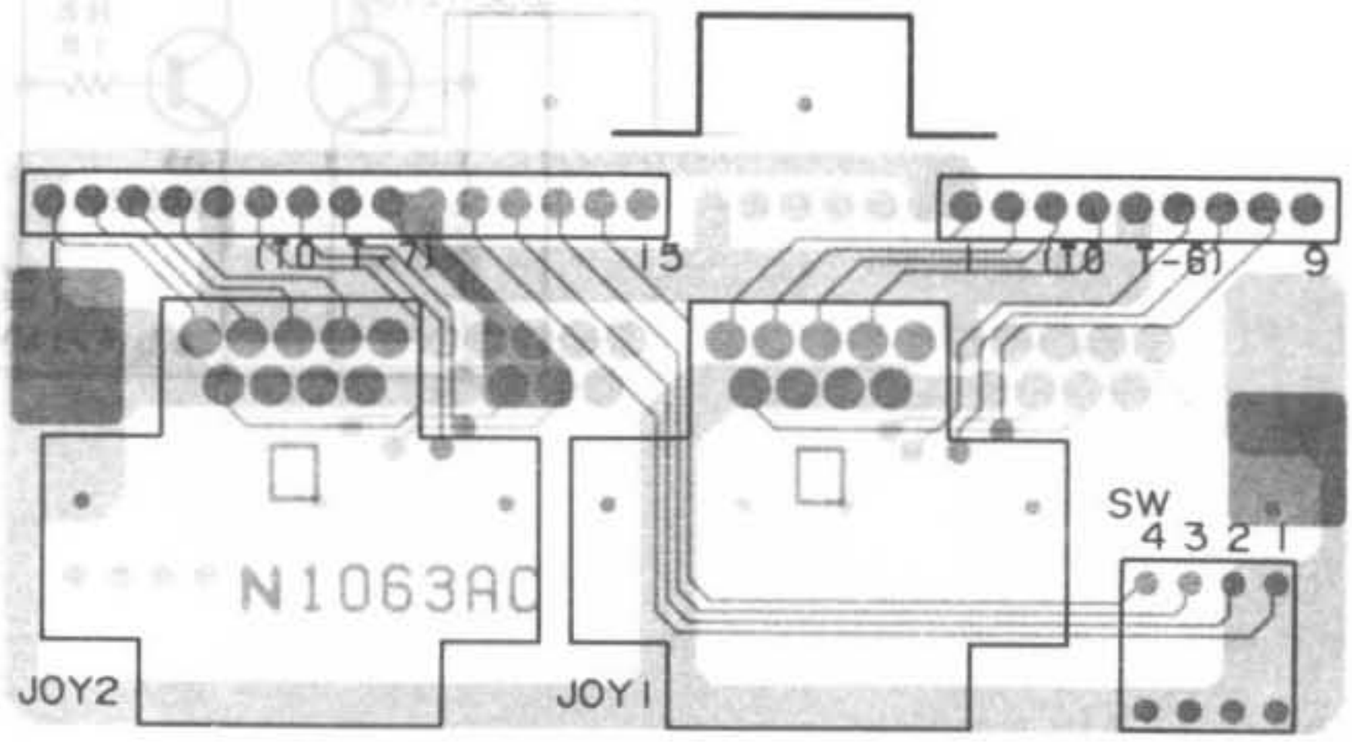
7 8 9 10 11 12

MZ-1E20 LAYOUT

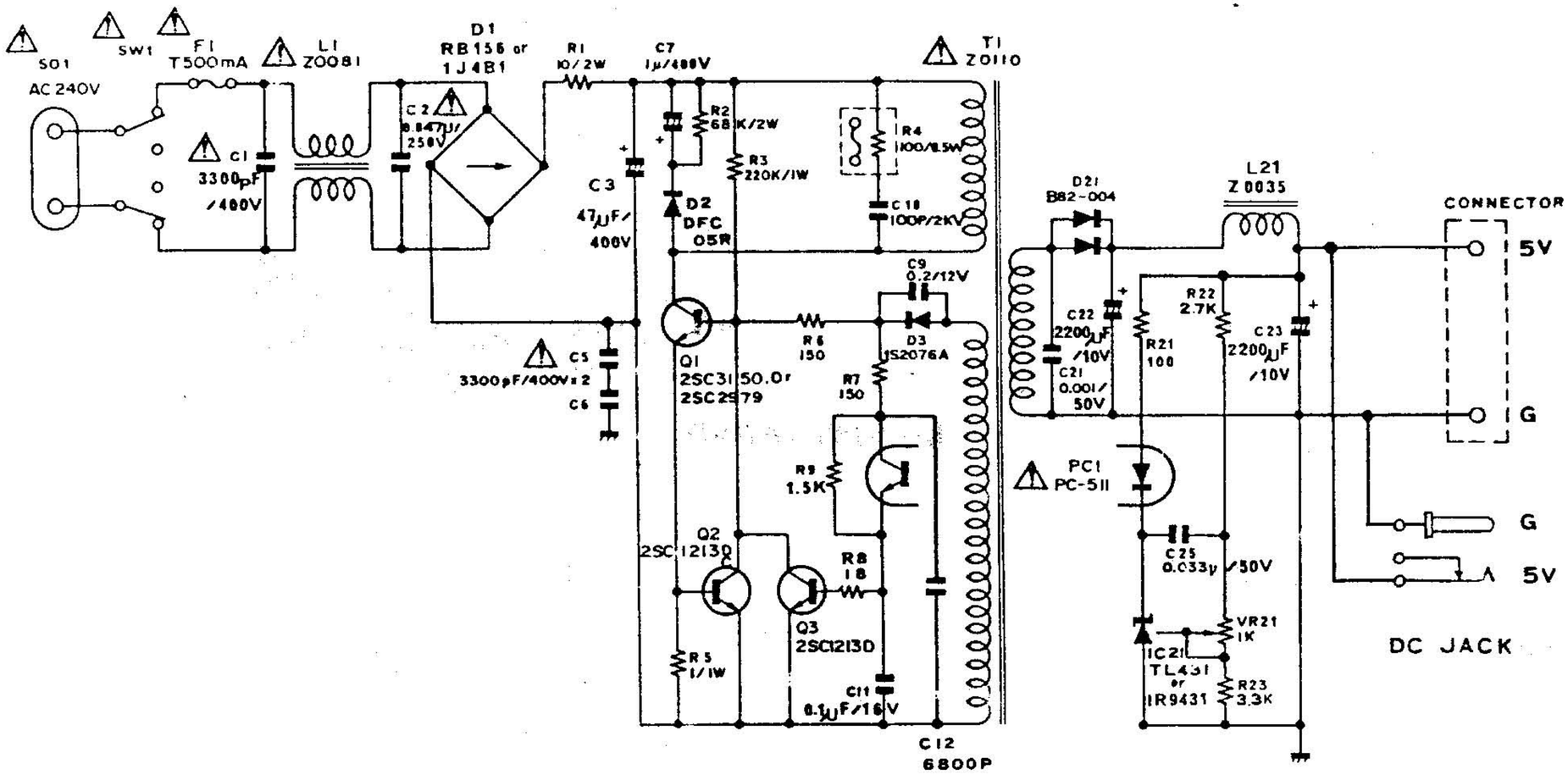


A B C D E F G H

JOY STICK LAYOUT



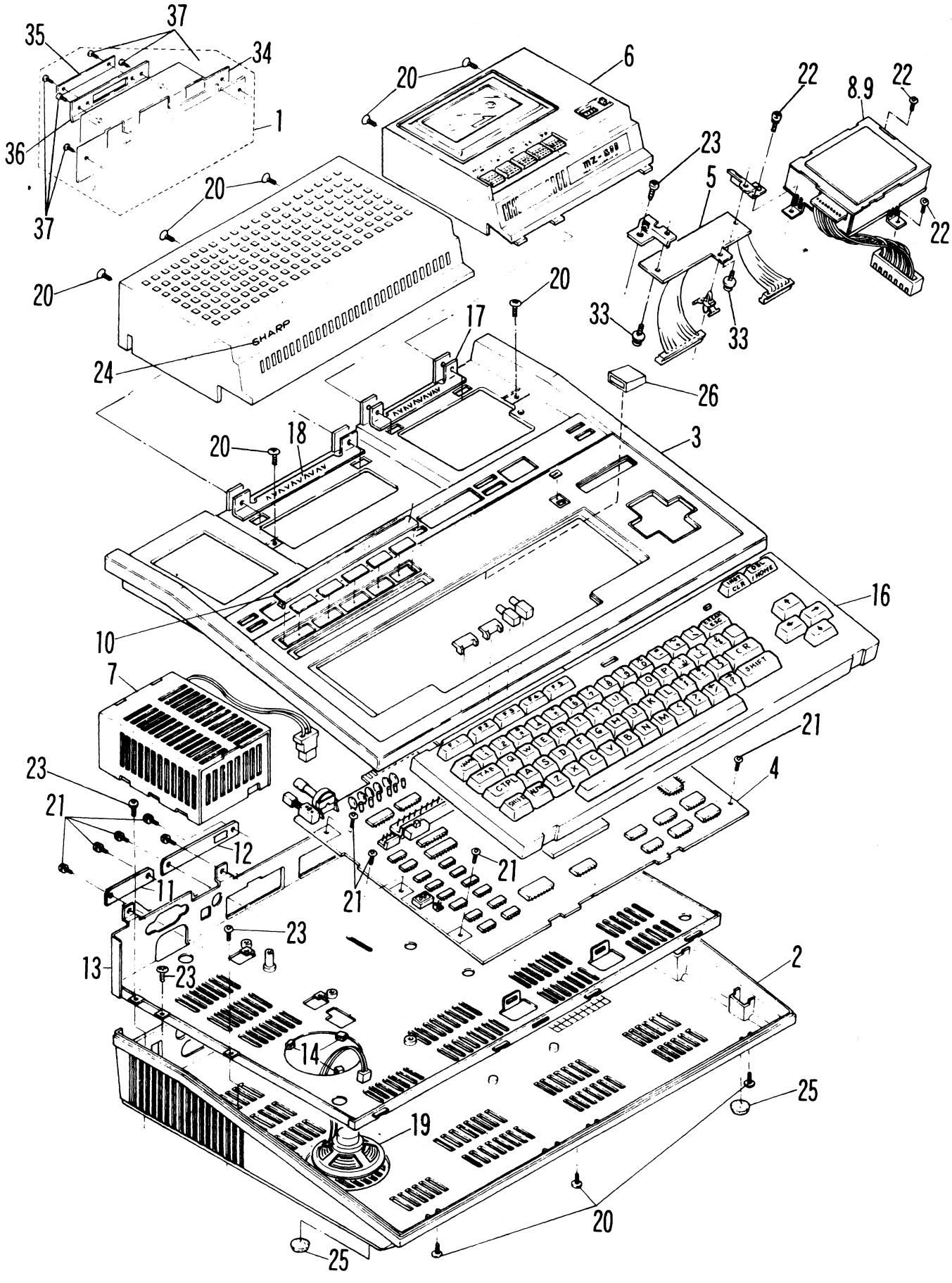
Power Supply Circuit



1 CPU Unit Exteriors

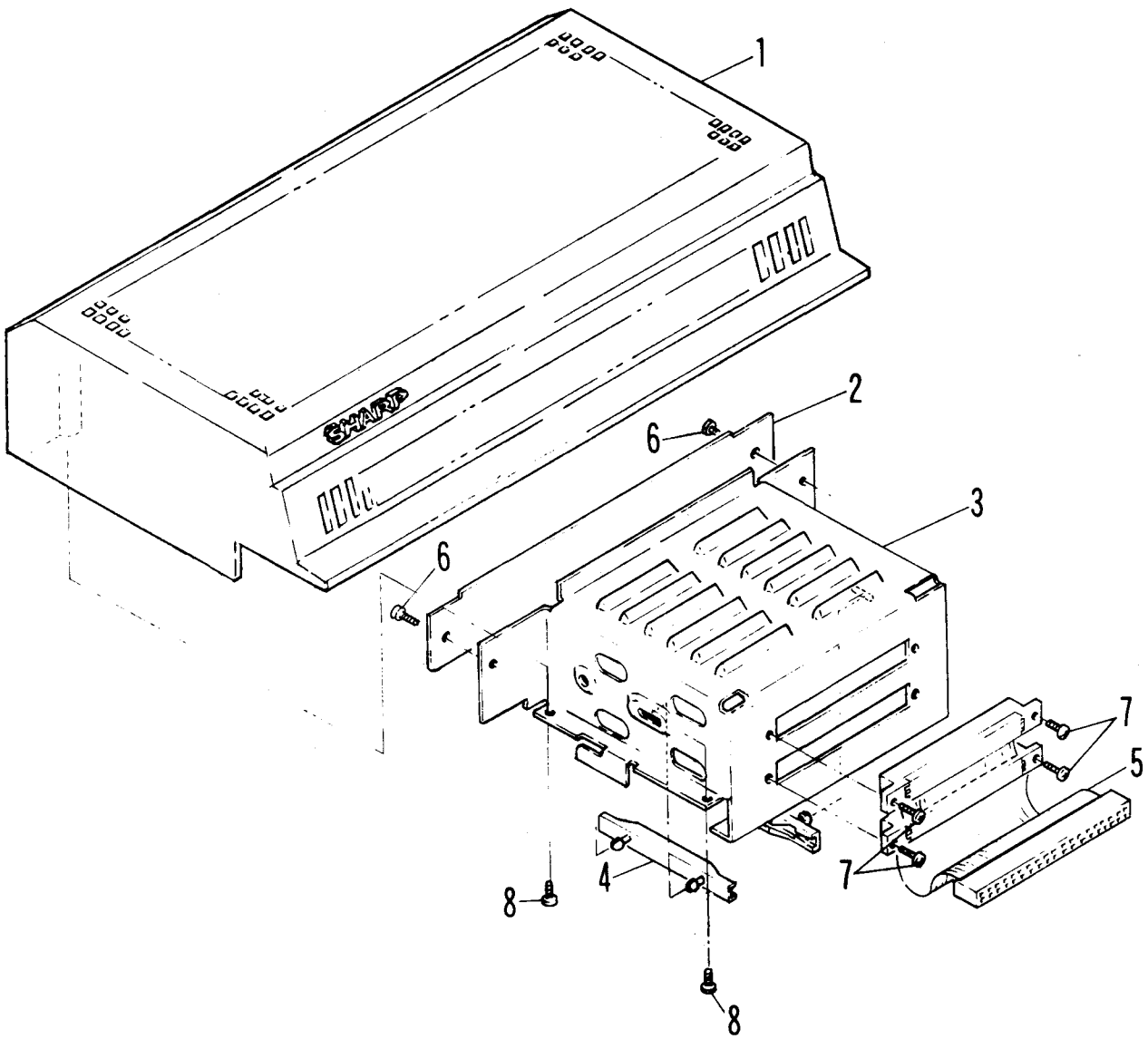
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCÖVH1002ACZB	AQ		D	I/O Cover unit
2	DUNTG1412ACZZ	AX		D	Bottom cabinet
3	DUNTG1413ACZZ	AX		D	Top cabinet
4	DUNTK1418ACZZ	**	N	C	CPU PWB Unit
5	DUNTK1419ACZZ	BA	N	C	Joy PWB Unit
6	DUNT-1409ACZZ	BS		B	Cassette unit
7	DUNT-1420ACZZ	BM	N	E	Power supply unit
8	DUNT-1421ACZZ	BM	N	E	RF Modulator (Europe except France)
9	DUNT-1435ACZZ	BK		E	RF Modulator (France only)
10	GCÖVH1002ACZZ	AB		D	Aclyric cover
11	GFTAR1019ACZZ	AB		D	Lid for 26P connector
12	GFTAR1025ACZZ	AC		D	Lid for joy connector
13	LCHSM1018ACZZ	AY		C	Main chassis
14	PCUSS1002ACZZ	AA		C	Speaker cushion
15	QCNCW1008AC03	AC		C	Connector
16	QSW-K1031ACZZ	BH		C	Key board unit
17	QTANS1002ACZZ	AD		C	Ground terminal
18	QTANS1003ACZZ	AD		C	Ground terminal
19	VSP0080P-608N	AN		B	Speaker (P008P)
20	XBBSC30P10000	AA		C	Screw (3×10)
21	XBPSM30P06KS0	AA		C	Screw (3×6KS)
22	XBPSM30P08K00	AA		C	Screw
23	XUPSD30P10000	AA		C	Screw (3×10)
24	HBDGB1003ACZZ	AC		D	"Sharp" badge
25	GLEGG1020CCZZ	AD		D	Rubber foot
26	PGUMS1266CCZZ	AA		C	Cushion for PWB fixing angle
27	LANGT1077ACZZ	AC		C	Angle for PWB
28	LANGT1078ACZZ	AC		C	Angle for PWB
29	QCNCM1056ACZZ	AG		C	Connector
30	QCNW-1111ACZZ	AK		C	Cable (15pin)
31	QCNW-1112ACZZ	AG		C	Cable (9pin)
32	QSW-Z1032ACZZ	AM	N	B	Dip switch (4pin)
33	XBPSM30P06KS0	AA		C	Screw (3×6KS)
34	GCÖVH1009ACZB	AN		D	I/O Cover
35	GFTAR1021ACZB	AE		D	Lid
36	HPNLC1004ACZB	AE		D	I/O Panel
37	XBBSC30P06000	AA		C	Screw (3×6)

1 CPU Unit Exteriors



2 I/O Cabinet Unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCABB1018ACZB	AS		D	I/O Cabinet unit
2	GFTAR1024ACZA	AF		D	Lid for slot
3	LCHSM1010ACZZ	AQ		C	I/O Chassis
4	LHLDZ1005ACZZ	AD		C	PWB guide
5	QCNW-1076ACZZ	BA		C	Cable with conector (for 44pin)
6	XBBSC30P06000	AA		C	Screw (3×6)
7	XBPSD30P10KS0	AB		C	Screw (3×10KS)
8	XUPSD30P08000	AA		C	Screw (3×8)



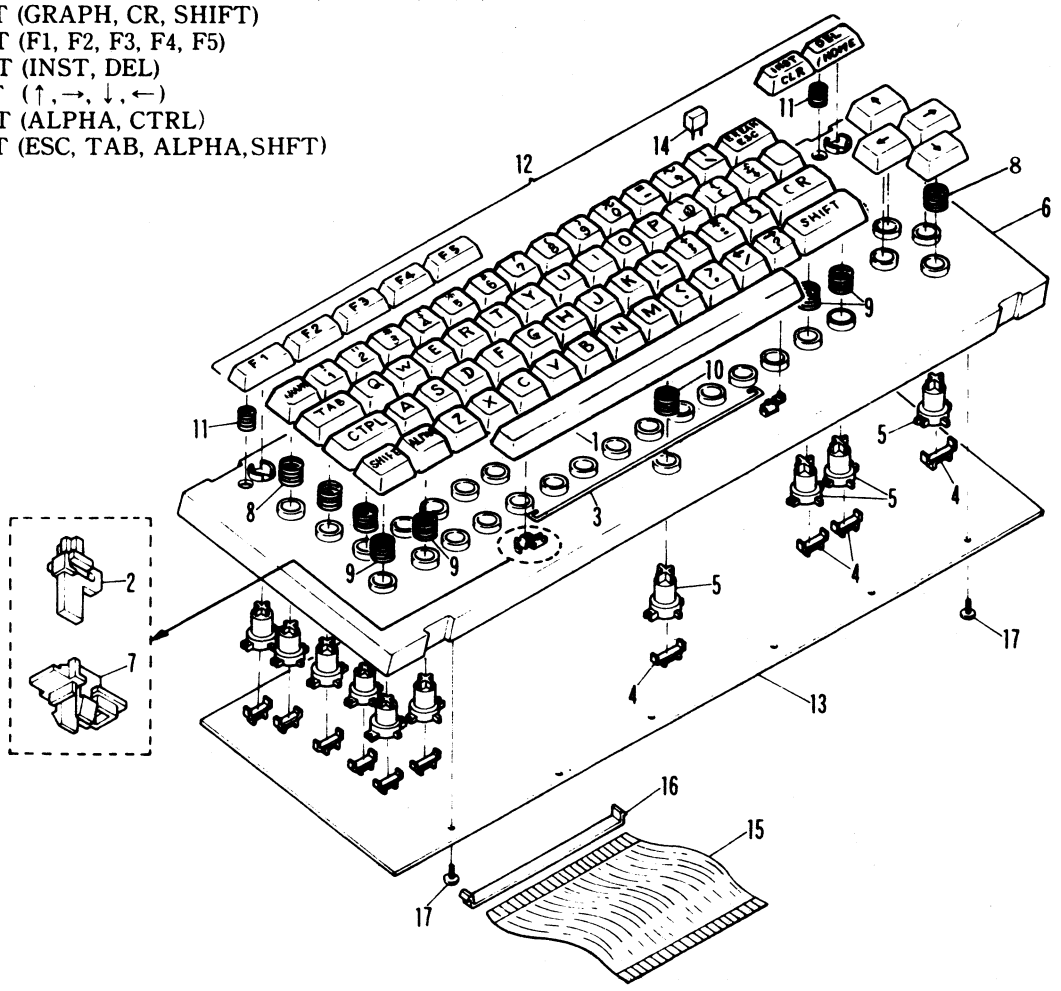
3 CPU Board Unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LBSHZ2029SCZZ	AB		C	Bushing
2	QCNCM1009ACZB	AA		C	Connector (2pin)
3	QCNCM1009ACZi	AC		C	Connector (9pin)
4	QCNCM1009ACZL	AC		C	Connector for Colour encoder (12pin)
5	QCNCM1009ACZÖ	AC		C	Connector (15pin)
6	QCNCM1010ACZZ	AF		C	Connector for Power supply (For power supply)
7	QCNCW1013ACZZ	AC		C	Connector for Recorder (For data recorder)
8	QCNCM1038ACZZ	AM		C	Connector (JAE 50P)
9	QCNCW1270CC2J	AE		C	Connector for Key
10	QJAKC1013CCZZ	AC		B	Jack (for MIC)
11	QSÖCZ6418ACZZ	AD		C	IC socket (18pin)
12	QSÖCZ6428ACZZ	AE		C	IC socket (28pin)
13	QSÖCZ6440ACZZ	AG		C	IC socket (40pin)
14	QSW−P1009ACZZ	AF		B	Push switch (Reset)
15	RCRS−1007ACZZ	AV		B	X−TAL (17.7344MHz)
16	RMPTCB102QCKB	AD		B	Block resistor (1.0KΩ×12 1/8W ±10%)
17	RMPTC8103QCKB	AD		B	Block resistor (10KΩ×8 1/8W ±10%)
18	RVR−B1450QCZZ	AE		B	Variable resistor
19	VCEAAU1AW107Q	AB		C	Capacitor (10V 100μF 6.5φ×10)
20	VCEAAA1AW227M	AC		C	Capacitor (10WV 27μF)
21	VCEAAU1EW475Q	AB		C	Capacitor (25WV 4.7μF)
22	VCTYPU1EX223M	AB		C	Capacitor (25WV 0.022μF)
23	VCTYPU1EX333M	AB		C	Capacitor (25WV 0.033μF)
24	VCTYPU1EX473M	AB		C	Capacitor (25WV 0.047μF)
25	VHiD65040−032	BT		B	IC
26	VHiLH0080A/−1	AX		B	LSI (LH0080A)
27	VHiLH0081A/−1	AW		B	LSI (LH0081A)
28	VHiLM386N//−1	AH		B	IC
29	VHiMB81416−12	AZ		B	LSI (MB81416−12)
30	VHiNE556N//−1	AH		B	IC (NE556N)
31	VHiUPD8255/−1	AV		B	LSI (UPD8255)
32	VHi27128/AC85	BP		B	P−ROM
33	VHi8253////−1	BA		B	LSI (8253)
34	VS2SC458K//−1	AC		B	Transistor (2SC458K)
35	VCCCPU1HH101J	AB		C	Capacitor (50WV 100pF)
36	VCEAAU1CW106Q	AB		C	Capacitor (16WV 10μF)
37	VCEAAA1CW226Q	AB		C	Capacitor (16WV 22μF)
38	VCEAAU1HW105Q	AB		C	Capacitor (50WV 1.0μF)
39	VCKYPU1HB102K	AA		C	Capacitor (50WV 1000pF)
40	VCSATA1CE226M	AB		C	Capacitor (16WV 22μF)
41	VCSATA1CE336M	AB		C	Capacitor (16WV 33μF)
42	VCTYPU1EX103M	AB		C	Capacitor (25WV 0.01μF)
43	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
44	VHDDS1588L1−1	AD		B	Diode (DS1588L1)
45	VHiCD4069B/−1	AE		B	IC
46	VHiM74LS00/−1	AE		B	IC (M74LS00)
47	VHiM74LS02/−1	AE		B	IC (M74LS02)
48	VHiM74LS04/−1	AE		B	IC (M74LS04)
49	VHiM74LS08/−1	AE		B	IC (M74LS08)
50	VHiM74LS125−1	AH		B	IC (M74LS125)
51	VHiM74LS14/−1	AM		B	IC (M74LS14)
52	VHiM74LS145−1	AH		B	IC
53	VHiM74LS245−1	AM		B	IC (M74LS245P)
54	VHiM74LS257−1	AQ		B	IC (M74LS257P)
55	VHiM74LS32/−1	AF		B	IC (M74LS32)
56	VHiM74LS365−1	AF		B	IC (M74LS365P)
57	VHiM74LS74/−1	AG		B	IC (M74LS74)
58	VHiM74LS86/−1	AF		B	IC (M74LS86P)
59	VHiSN74LS373N	AL		B	IC (SN74LS373)
60	VHiSN7417N/−1	AG		B	IC (SN7417N)
61	VHiSN76489/−1	AW		B	IC
62	VHi4164−150−H	AZ		B	IC (4164)
63	VRD−ST2EY000J	AA		C	Resistor (1/4W ±5%)
64	VRD−ST2EY100J	AA		C	Resistor (1/4W 10Ω ±5%)
65	VRD−ST2EY101J	AA		C	Resistor (1/4W 100Ω ±5%)
66	VRD−ST2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%)
67	VRD−ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
68	VRD−ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
69	VRD−ST2EY122J	AA		C	Resistor (1/4W 1.2KΩ ±5%)
70	VRD−RV2EY152J	AA		C	Resistor (1/4W 1.5KΩ ±5%)
71	VRD−ST2EY182J	AA		C	Resistor (1/4W 1.8KΩ ±5%)
72	VRD−ST2EY183J	AA		C	Resistor (1/4W 18KΩ ±5%)
73	VRD−ST2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)
74	VRD−ST2EY330J	AA		C	Resistor (1/4W 33Ω ±5%)
75	VRD−ST2EY331J	AA		C	Resistor (1/4W 330Ω ±5%)
76	VRD−ST2EY332J	AA		C	Resistor (1/4W 3.3KΩ ±5%)
77	VRD−ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
78	VRD−ST2EY473J	AA		C	Resistor (1/4W 47KΩ ±5%)
79	VRD−ST2EY561J	AA		C	Carbon resistor (1/4W 560Ω ±5%)
80	VRD−ST2EY683J	AA		C	Resistor (1/4W 68KΩ ±5%)

4 Key Board Unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0CFD5799D////	AF		C	Space key
2	0CF33623A/////	AB		C	Crank guide F
3	0CF33633A/////	AD		C	Crank shaft A
4	0CF63033A/////	AC		C	Key contact
5	0CF33357A/////	AA		C	Guide tip
6	0CF49063A/////	AX		C	Frame (NSH−1)
7	0CF33611A/////	AB		C	Crank holder F
8	0CF33644A/////	AA		C	Return spring (for 60 key)
9	0CF33648A/////	AA		C	Return spring (for shift key)
10	0CF33644C/////	AA		C	Return spring (for space key)
11	0CF07111C/////	AA		C	Return spring (for harf key)
12	0CF42744A/////	BE	N	C	Key top set A
13	0CF63877C/////	BB	N	E	PWB W. Parts
14	0CF17311F/////	AF	N	B	LED
15	0CF49884A/////	AN		C	Flat cable
16	0CF49764A/////	AC		C	Protector
17	XBTSD20P06000	AA		C	Screw
18	0CF42744B/////	AT	N	C	Key top set B
19	0CF42744C/////	AT	N	C	Key top set C
20	0CF42744D/////	AD	N	C	Key top set D
21	0CF42744E/////	*AT	N	C	Key top set E
22	0CF42744F/////	AH	N	C	Key top set F
23	0CF42744G/////	AK	N	C	Key top set G
24	0CF42744H/////	AF	N	C	Key top set H
25	0CF42744J/////	AH	N	C	Key top set J
26	0CF42744K/////	AD	N	C	Key top set K
27	0CF42744L/////	AH	N	C	Key top set L
28	0CFD5000D////	AG		C	Blank key top

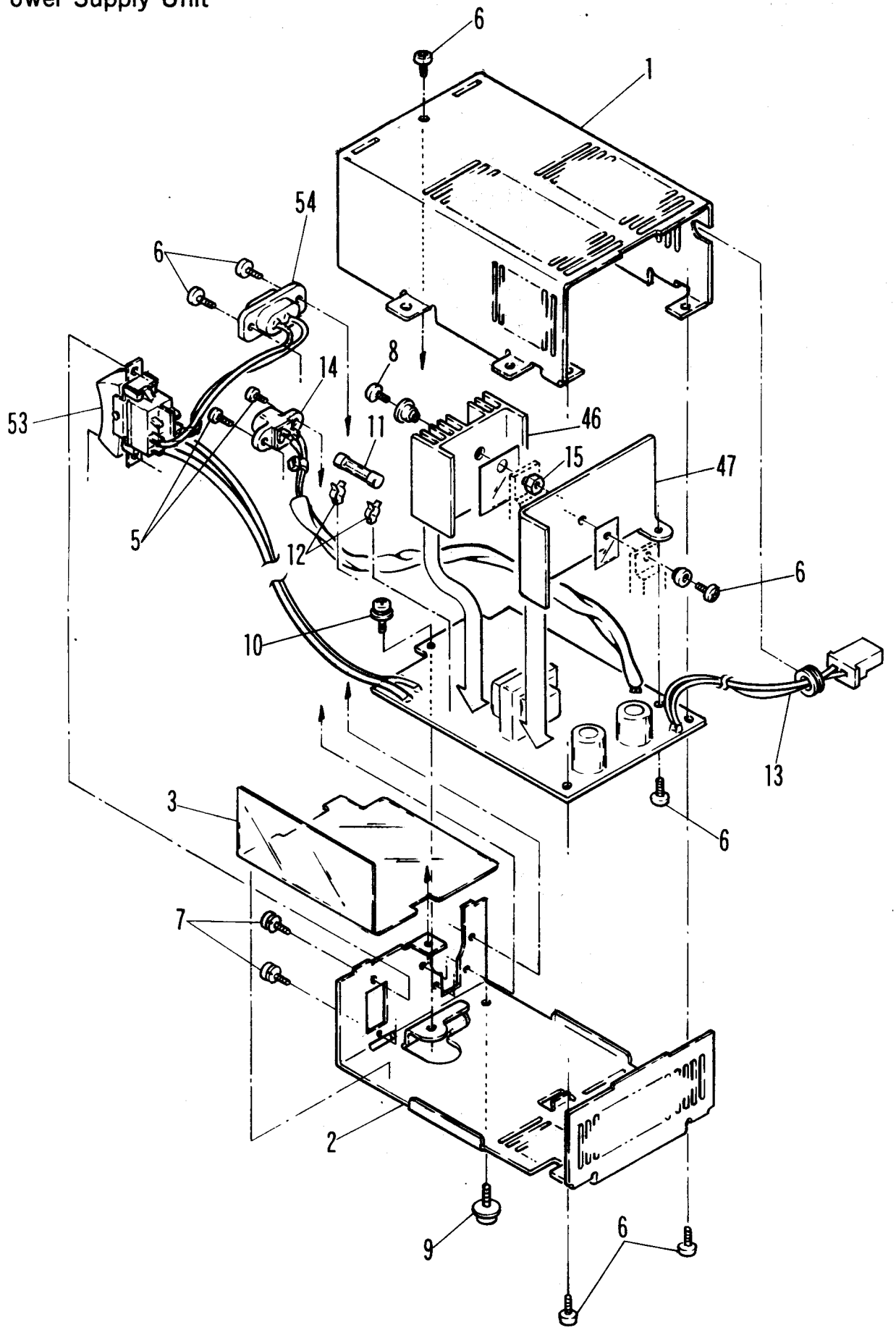
* Key top unit
B UNIT (1~9, 0, *, ↑, −, ↑, \, Q, W, E)
C UNIT (M, N, V, C, X, Z, L, K, J, H, F, S, I, U, Y, T)
D UNIT (?)
E UNIT (R, O, P, A, D, G, B, @, 〔, ; , : , 〕, ’, ・, /, ↓)
F UNIT (GRAPH, CR, SHIFT)
G UNIT (F1, F2, F3, F4, F5)
H UNIT (INST, DEL)
J UNIT (↑, →, ↓, ←)
K UNIT (ALPHA, CTRL)
L UNIT (ESC, TAB, ALPHA, SHFT)



5 Power Supply Unit

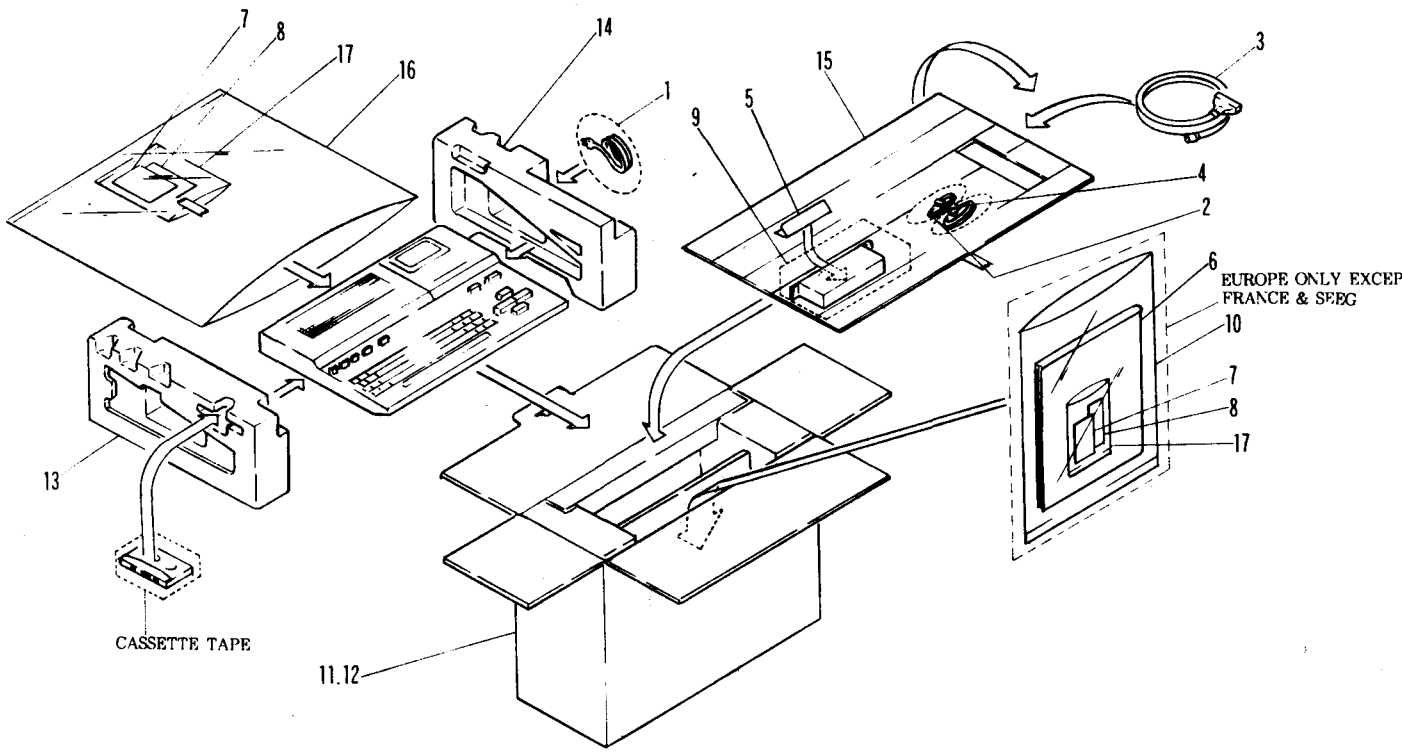
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	PCÖVS0181VAZZ	AG		C	Case (B)	
2	PCÖVS0215PAZZ	AF		C	Case (A)	
3	PZETi0021PAZZ	AE		C	Barrier	
4	LBNDC0008PAZZ	AA		C	Wire band	
5	XBBSM20P06000	AA		C	Screw (2×6)	
6	XBBSC30P06000	AA		C	Screw (For heat sink INLET)(3×6)	
7	XBPSC30P06K00	AA		C	Screw (For switch)(3×6)	
8	XBPSD30P08000	AA		C	Screw (For heat sink)	
9	XBPSD40P08KS0	AA		C	Screw (4P×8S)	
10	XBPSC30P06KS0	AA		C	Screw (3P×6S)	
⚠ 11	QFS−C0002PAZZ	AD		A	Fuse	[F1]
12	QFSHA0001PAZZ	AA		C	Fuse holder (H−0011)	
13	DSÖCN0344PAZZ	AF		C	Connector (out put) W.Wire	
14	QJAKC0004PAZZ	AD		C	Jack (For DC)	
15	XNESD30−24000	AA		C	Nut (For heat sink)	
16	RTRNZ0035PAZZ	AE	N	B	Filter coil	[L21]
⚠ 17	RTRNZ0110PAZZ	AT		B	Transformer	[T1]
⚠ 18	RTRNZ0081PAZZ	AH		C	Filter	[L1]
19	RVR−M0089PAZZ	AC		B	Variable resistor (1KΩ)	[VR21]
20	VHDRB156///−1	AG		B	Diode	[D1]
21	RH−iX0464PAZZ	AF		B	IC	[IC21]
22	VRD−RU2EE152J	AA		C	Resistor (1/4W 1.5KΩ ±5%)	[R9]
23	VRD−SC2EF180J	AA		C	Resistor (1/4W 18Ω ±5%)	[R8]
24	VRD−SC2EF151J	AA		C	Resistor (1/4W 150Ω)	[R6]
⚠ 25	RC−FZ030CPAZZ	AE		C	Capacitor	[C2]
26	VRD−RU2EE151J	AA		C	Resistor (1/4W 150Ω)	[R7]
27	VRD−SC2EF272J	AA		C	Resistor (1/4W 2.7KΩ ±5%)	[R22]
⚠ 28	RC−QZ0023PAZZ	AD		C	Capacitor (AC400V 3300pF)	[C1,5,6]
29	RR−XZ0008PAZZ	AB		C	Resistor	[R4]
30	VCEAAU1AM228M	AC		C	Capacitor (10WV 2200μF)	[C22,23]
31	VCEAAU2GM105M	AD		C	Capacitor (400WV 1.0μF)	[C7]
32	VCEAAU2GM476Y	AH		C	Capacitor (400WV 47μF)	[C3]
33	VCKYPU1HB682K	AA		C	Capacitor (50WV 6800pF)	[C12]
34	VCKYPU1NB204Z	AB		C	Capacitor (12WV 0.20μF)	[C9]
35	VCKYPU3DB101K	AB		C	Capacitor (2000WV 100pF)	[C10]
36	VCQYKU1HM102K	AA		C	Capacitor (50WV 1000pF)	[C21]
37	VCQYKU1HM333K	AB		C	Capacitor (50WV 0.033μF)	[C25]
38	VCTYPG1CD104Z	AE		C	Capacitor (16WV 0.10μF)	[C11]
39	VHDDFC05R///−1	AC	N	B	Diode	[D2]
40	VHD1S2076A/−1	AB		B	Diode (1S2076A−FEC)	[D3]
41	VRD−ST3AF224J	AA		C	Resistor (1W 220KΩ ±5%)	[R3]
42	VRS−PT3AB1R0J	AA		C	Metal film resistor (1W 1Ω ±5%)	[R5]
43	VRS−PT3DB683J	AA		C	Resistor (2W 68KΩ ±10%)	[R2]
44	VRW−KT3DC100K	AC		C	Resistor (2W 10Ω ±10%)	[R1]
45	VS2SC1213−D1A	AC		C	Transistor	[Q2,3]
46	PRDAR0143PAZZ	AF		C	Heat sink	
47	PRDAR0144PAZZ	AE		C	Heat sink	
48	VHDESAC8204−2	AN		B	Diode	[D21]
49	VS2SC3150//−1	AK		C	Transistor	[Q1]
50	VRD−RU2EE101J	AA		C	Resistor (1/4W 100Ω)	[R21]
51	VRD−SC2EF332J	AA		C	Resistor (1/4W 3.3KΩ)	[R23]
52	RH−PX0075PAZZ	AK		B	Photo transistor	[PC1]
⚠ 53	QSW−C0003PAZZ	AK		B	AC switch	[SW1]
⚠ 54	QSÖCA0003PAZZ	AF		C	AC inlet	[SO1]

5 Power Supply Unit



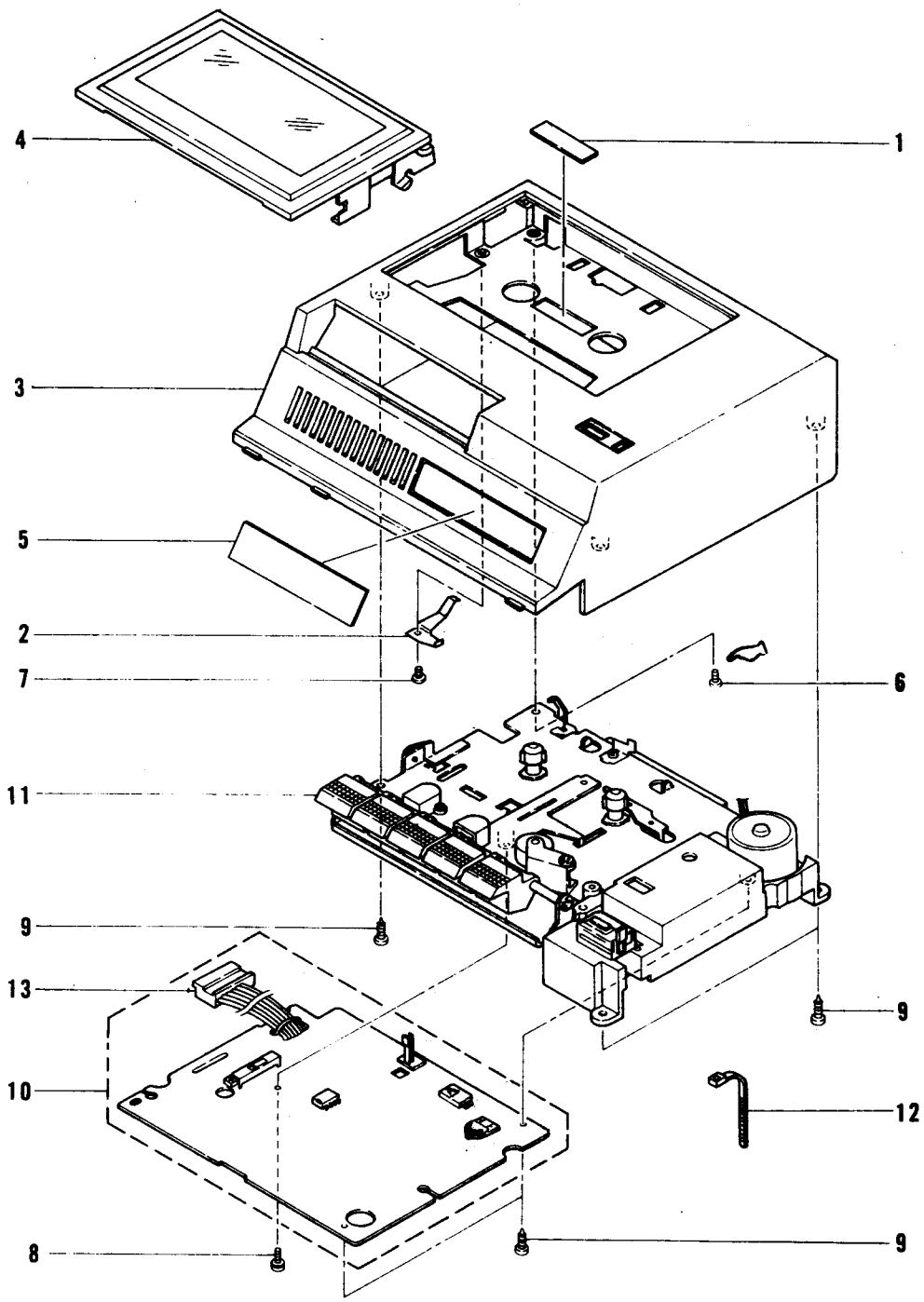
6 Packing Parts

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QACCZ3321QCN1	AL		C	AC cord (France only)
2	QACCE3620QCZZ	AL		D	AC cord (Europe except France)
3	QCNW-1065ACZZ	BA		D	Cable for TV (France only)
4	QCNW-1049ACZZ	AN		C	Cable for TV (Europe except France)
5	TINSM1294ACZZ	AC	N	D	Instruction manual (Supplement)
6	TINSG1212ACZZ	BE	N	D	Instruction manual Basic (Europe except France seeg)
7	TLABZ1010ACZZ	AD		D	Function label
8	TLABZ1102ACZZ	AD		D	Graphic label
9	SSAKA5004CCZZ	AA		D	Poly bag (100×300mm)
10	SSAKH0013HCZZ	AA		D	Poly bag (260×400mm)
11	SPAKC1556ACZZ	AQ	N	D	Packing case (France only)
12	SPAKC1552ACZZ	AQ	N	D	Packing case (Europe except France)
13	SPAKA1624ACZL	AH	N	D	Packing cushion L
14	SPAKA1624ACZR	AH	N	D	Packing cushion R
15	SPAKA1625ACZZ	AM	N	D	Packing sleeve (Accessories)
16	SSAKH0014HCZZ	AB		D	Poly bag (640×500mm)
17	SSAKA0231QCZZ	AA		D	Poly bag (80×220 30U)
18	RTPEK1006AC84	BB		D	Master cassette tape
19	TLABZ1103ACZZ	AA		D	Label (DC 5V)
20	TLABE1119ACZZ	AC		D	Label for tape (1Z016)
21	TLABE1120ACZZ	AC		D	Label for tape (1Z013)
	TLABZ1009ACZC	AA		D	Label
22	TLABS1128ACZZ	AB		D	Caution



7 Cassette Unit Exteriors

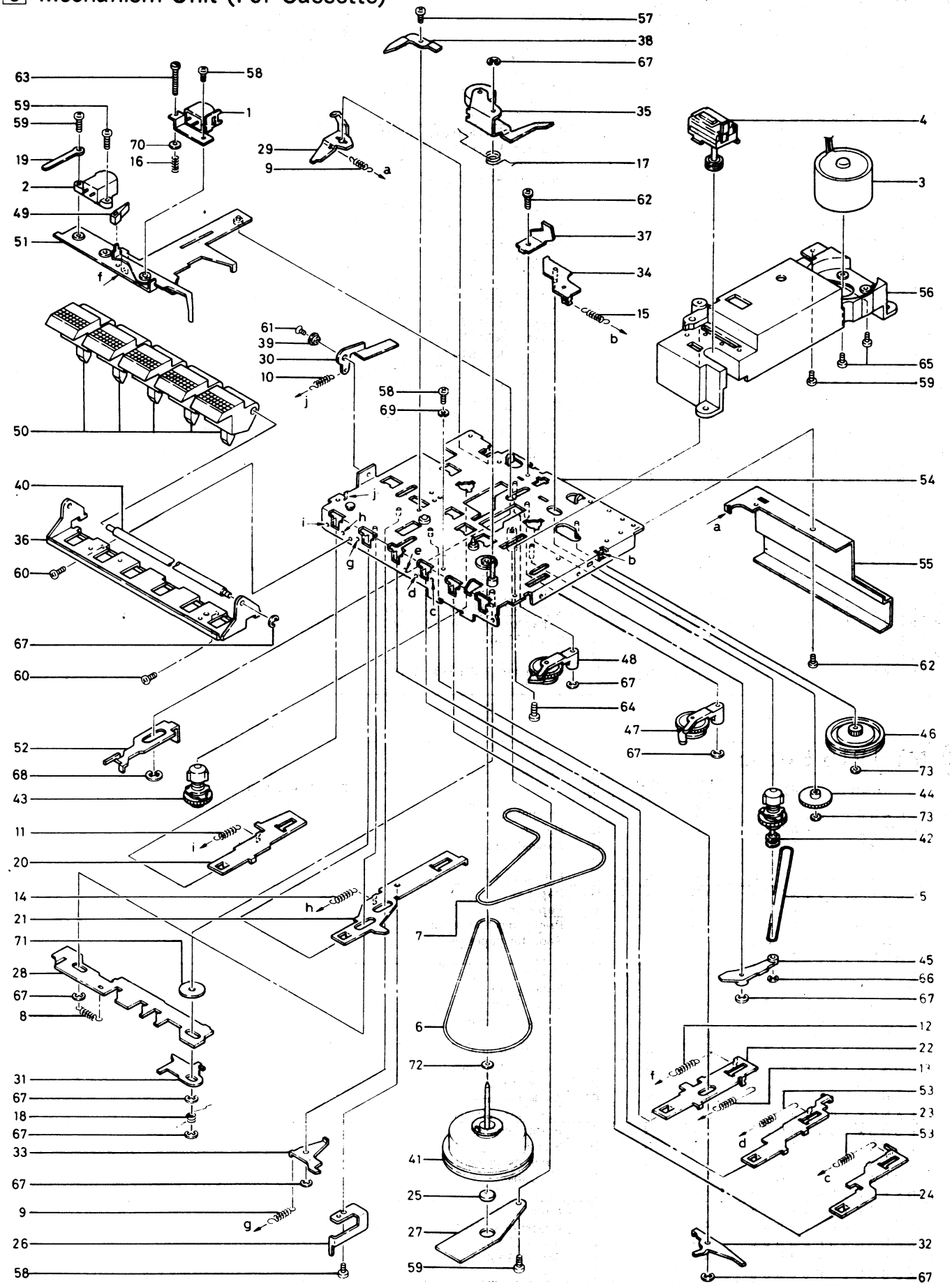
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0BV07571700 43	AA	N	D	Tape mirror
2	0BV66118200 02	AC	N	C	Cassette lid spring
3	0BV66880000 17	AT	N	D	Cabinet ass'y
4	0BV66880400 19	AL	N	D	Cassette lid ass'y
5	0BV66882200 15	AC	N	D	Plate
6	0BV97102604 14	AA		C	Screw (P2.6X4−SN)
7	0BV97112604 17	AA		C	Screw (T2.6X4−SN)
8	0BV97182605 11	AA	N	C	Screw (P2.6X5−SN−S)
9	0BV97602610 18	AA	N	C	Screw (TP2.6X10−SN−A)
10	0BV66800100 05	BG	N	E	Amp PWB unit
11	0BV66804000 17	BP	N	E	Mechanism ass'y
12	0BV06463100 06	AA	N	C	Lead wire clamp
13	0BV66854000 01	AG	N	C	Connector (9pin)



8 Mechanism Unit (For Cassette)

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0BV021068 0007	AN	N	B	Record−play back head
2	0BV021128 0006	AH	N	B	Erase head
3	0BV022283 0001	AW	N	B	Motor
4	0BV044080 0004	AM	N	B	Tape counter
5	0BV056069 0004	AD	N	B	Counter
6	0BV056080 0009	AD	N	B	Capstan belt
7	0BV056095 0005	AD		B	Gear belt
8	0BV063012 1009	AA	N	C	EXT spring
9	0BV063022 0009	AA		C	EXT spring
10	0BV063060 0007	AA		C	EXT spring
11	0BV063196 0001	AA		C	EXT spring
12	0BV063198 2009	AA	N	C	EXT spring
13	0BV063199 2002	AA	N	C	EXT spring
14	0BV063206 0005	AA	N	C	EXT spring
15	0BV063207 0008	AA	N	C	EXT spring
16	0BV063511 0000	AA		C	COM spring
17	0BV063697 3002	AA		C	SPL spring
18	0BV562415 0003	AF		C	Spring
19	0BV065338 0009	AA		C	Lead−wire clamper
20	0BV380129 0009	AC		C	Stop lever
21	0BV380131 1007	AD		C	Record lever
22	0BV380132 1000	AC		C	Play lever
23	0BV380133 1003	AC	N	C	Rewind lever
24	0BV380134 1006	AD	N	C	F.F. lever
25	0BV500170 0005	AA		C	Flywheel shaft supporter
26	0BV622180 0005	AC	N	C	Record switch spring
27	0BV650118 0009	AB		C	Flywheel Base
28	0BV650136 1006	AD	N	C	Lock plate
29	0BV650137 2000	AC	N	C	Safety lever
30	0BV650138 0001	AB		C	Eject arm
31	0BV650139 0004	AB		C	Stop arm
32	0BV650140 1009	AB	N	C	Reverse cue lever
33	0BV650141 3004	AB	N	C	Record lock lever
34	0BV650147 1000	AE		C	Take−up arm set
35	0BV650148 0002	AF		C	Pinch roller base ass'y
36	0BV650146 1007	AG		C	6 Push switch base
37	0BV650183 2003	AC		C	Push spring
38	0BV650184 1005	AC	N	C	Stopper spring
39	0BV650203 0006	AB		C	Arm support A
40	0BV650225 1005	AD	N	C	Switch shaft
41	0BV650230 0505	AK	N	C	Flywheel
42	0BV650258 4000	AF	N	C	Take−up reel base ass'y
43	0BV650259 5004	AF	N	C	Reel base ass'y A
44	0BV650262 0009	AB		C	Take−up gear
45	0BV650266 0001	AB		C	Take−up lever
46	0BV650275 2001	AG	N	C	Clutch ass'y
47	0BV650292 0002	AF	N	C	Rewind arm ass'y
48	0BV650293 0005	AF	N	C	First foward arm ass'y
49	0BV650294 0008	AA	N	C	Tension pick up
50	0BV662862 0024	AD	N	C	Push button
51	0BV666105 0008	AG	N	C	Head base ass'y
52	0BV666141 0000	AB	N	C	Switch lever
53	0BV667400 0003	AA	N	C	EXT Spring
54	0BV668100 0005	AS	N	C	Mechanism chassis ass'y
55	0BV668120 0007	AE	N	C	Angle
56	0BV668270 0005	AG	N	C	Motor support
57	0BV971020 0254	AA	N	C	Screw (P2X2−SK)
58	0BV971020 0313	AA		C	Screw (P2X3−SN)
59	0BV971020 0416	AA		C	Screw (P2X4−SN)
60	0BV971020 0519	AA		C	Screw (P2X5−SN)
61	0BV971220 0412	AA		C	Screw (L2X4−SN)
62	0BV971820 0410	AA		C	Screw (P2X4−SN−S)
63	0BV974355 1004	AA		C	Screw (P2X10−SN)
64	0BV976026 0811	AA		C	Screw (Self tapp TP2.6X8−SN−A)
65	0BV979902 4006	AA	N	C	Screw (P2X4.7−SN)
66	0BV981101 5142	AA		C	E Type ring (ZR1.5−SU)
67	0BV981102 5145	AA		C	E Type ring (ZR2.5−SU)
68	0BV981103 0143	AA		C	E Type ring (ZR3−SU)
69	0BV986202 0115	AA	N	C	E Type ring (SW2−SN)
70	0BV987000 3003	AA		C	Washer (W021060030SN)
71	0BV987001 2005	AA	N	C	Washer (W030100080SN)
72	0BV987400 2004	AA		C	Washer (W021045025)
73	0BV987402 6004	AA		C	Washer (WP012036025)

8 Mechanism Unit (For Cassette)



9 PWB Unit (For Cassette)

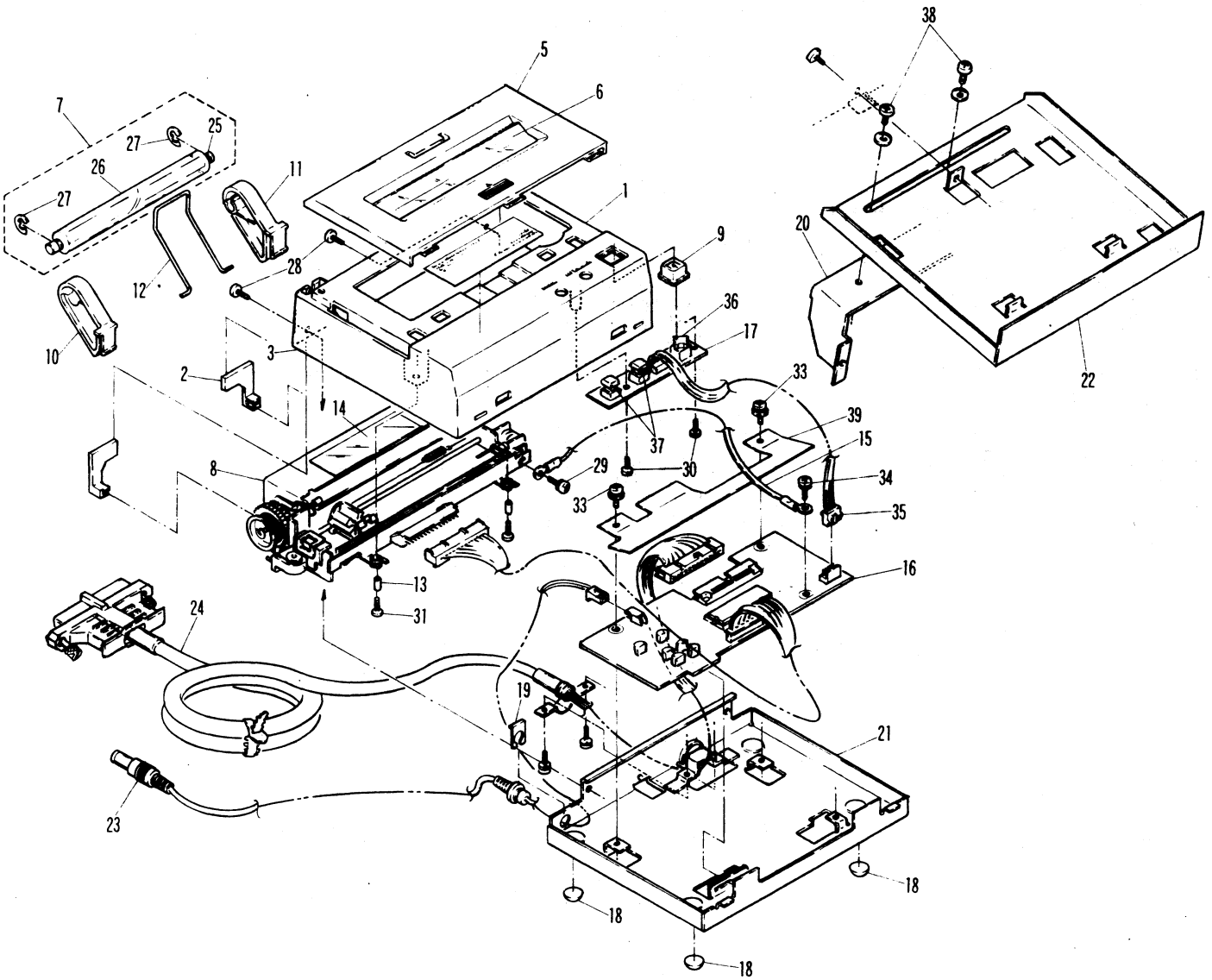
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0BV0364180002	AH		B	Slide SW [SW1~SW1-3]
2	0BV0365800008	AF	N	B	Leaf SW [SW2]
3	0BV9020046250	AF	N	B	Transistor (2SC2120-Y) [Q3,Q4]
4	VHDDS1588L2-1	AB		B	Diode [D1~D4]
5	0BV9110340008	AK	N	B	IC (μPC1470P) [IC2]
6	0BV9205118149	AA	N	C	Resistor (RD14D181J 180Ω) [R20]
7	0BV9208610248	AA	N	C	Resistor (RD16T102JT 1KΩ) [R21,R6]
8	0BV9208610341	AA	N	C	Resistor (RD16T103JT 10KΩ) [R18,10,9,7,13,15,28]
	0BV9208610341	AA	N	C	Resistor (RD16T103JT 10KΩ) [R27]
9	0BV9208615140	AA	N	C	Resistor (RD16T151JT 150Ω) [R19]
10	0BV9208615346	AA	N	C	Resistor (RD16T153JT 15KΩ) [R3]
11	0BV9208615449	AA	N	C	Resistor (RD16T154JT 150KΩ) [R11]
12	0BV9208620540	AA	N	C	Resistor (RD16T205JT) [R14]
13	0BV9208622243	AA	N	C	Resistor (RD16T222JT 22KΩ) [R12]
14	0BV9208622346	AA	N	C	Resistor (RD16T223JT 22KΩ) [R16]
15	0BV9208622449	AA	N	C	Resistor (RD16T224JT 220KΩ) [R1]
16	0BV9208627145	AA	N	C	Resistor (RD16T271JT 270Ω) [R30]
17	0BV9208633144	AA	N	C	Resistor (RD16T331JT 330Ω) [R22]
18	0BV9208647048	AA	N	C	Resistor (RD16T470JT 47Ω) [R2]
19	0BV9208647141	AA	N	C	Resistor (RD16T471JT 470Ω) [R26]
20	0BV9208647347	AA	N	C	Resistor (RD16T473JT 47KΩ) [R23,R4]
21	0BV9208656040	AA	N	C	Resistor (RD16T560JT 56Ω) [R8]
22	0BV9208656246	AA	N	C	Resistor (RD16T562JT 5.6KΩ) [R17]
23	0BV9208656442	AA	N	C	Resistor (RD16T564JT 560KΩ) [R29]
24	0BV9208682148	AA	N	C	Resistor (RD16T821JT 820Ω) [R31]
25	0BV9208682241	AA	N	C	Resistor (RD16T822JT 8.2KΩ) [R24]
26	0BV9227120142	AC	N	C	Resistor (RNP14T201JS 200Ω) [R32]
27	0BV9250347046	AB	N	C	Resistor (RS08AB3A470J 47Ω 1W) [R25]
28	0BV9298020174	AD	N	C	Variable resistor (PD8H3C201N 200Ω) [VR1]
29	0BV9318310250	AC	N	C	Capacitor (CD45X1E102K) [C2,5]
30	0BV9318347359	AC	N	C	Capacitor (CD45X1E473K) [C10]
31	0BV9349010161	AD	N	C	Capacitor (CE04W0J101MU) [C9]
32	0BV9349022063	AC		C	Capacitor (CE04W0J220MU) [C7]
33	0BV9349047064	AD	N	C	Capacitor (CE04W0J470MU) [C8]
34	0BV9349210060	AC		C	Capacitor (CE04W1C100MU) [C3]
35	0BV9349501061	AC		C	Capacitor (CE04W1H010MU) [C6]
36	0BV9349510960	AC		C	Capacitor (CE04W1HR10MU) [C4,C1,C11]
37	0BV9905210051	AD	N	C	Coil (55100K) [L1]
38	VHiUPC358C/-1	AG		B	IC [IC1]
39	0BV9020045558	AD	N	B	Transistor (2SC1815-GR) [Q1,Q2,Q5]

10 MZ-1P16 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCABB1006ACZA	AM	N	D	Cabinet top
2	GCABB1008ACZB	AC		C	Holder
3	GCABB1008ACZC	AL	N	D	Cabinet top
4	CFTAT1001ACZA	AK	N	D	Lid
5	GFTAT1009ACZA	AE	N	D	Lid for pen change
6	PCUT-1001ACZA	AD	N	D	Paper cut
7	CSFTZ1001ACZZ	AH		E	Paper shaft unit
8	DUNTM1051ACZZ	BW		E	Printer mechanism unit
9	JKNBZ1005AC02	AG	N	D	Knob for paper feed
10	LHLDZ1002ACL2	AB	N	D	Holder
11	LHLDZ1002ACR2	AB	N	D	Holder
12	PGiDW1001ACZZ	AB		D	Paper guide
13	PSPAB1003ACZZ	AA		C	Collar for printer
14	PZETE1005ACZZ	AA		C	Insulator sheet
15	QCNW-1013ACZZ	AD		C	Ground wire
16	DUNTK1425ACZZ	BF	N	E	CPU PWB unit
17	DUNTK1426ACZZ	AL	N	E	Switch PWB unit
18	GLEGP1001CCZZ	AB		C	Lubber foot
19	LANGT1079ACZZ	AB	N	C	Angle for cable
20	LANGK1082ACZZ	AH	N	C	Angle for sulaider
21	LCHSM1016ACZZ	AM	N	C	Bottom chassis
22	LCHSM1017ACZZ	AQ	N	D	Stand
23	QCNW-1108ACZZ	AL	N	C	Cable for power
24	QCNW-1109ACZZ	BD	N	C	I/F Cable
25	NSFTZ1001ACZA	AC		C	Paper holder
26	NSFTZ1001ACZB	AG		C	Paper shaft
27	XRESJ40-06000	AA		C	E type ring (4mm)
28	XBBSC30P06000	AA		C	Screw (3×6)
29	XBPSD30P04K00	AA		C	Screw (3×4K)
30	XUBSD26P08000	AA		C	Screw
31	XUBSD26P10000	AA		C	Screw
32	XBPSM30P06KS0	AA		C	Screw (3×6KS)

10 MZ-1P16 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
33	XBPSM30P08K00	AA		C	Screw
34	QCNW-1110ACZZ	AE	N	C	Connector (4pin)
35	QSW-P1010ACZZ	AC		C	Push switch (Paper feed)
36	QSW-P1011ACZZ	AD		C	Push switch (Pen Change,Reset)
37	LX-BZ0038FCZZ	AA		C	Screw
38	PZETV1010ACZZ	AC	N	C	Insulator



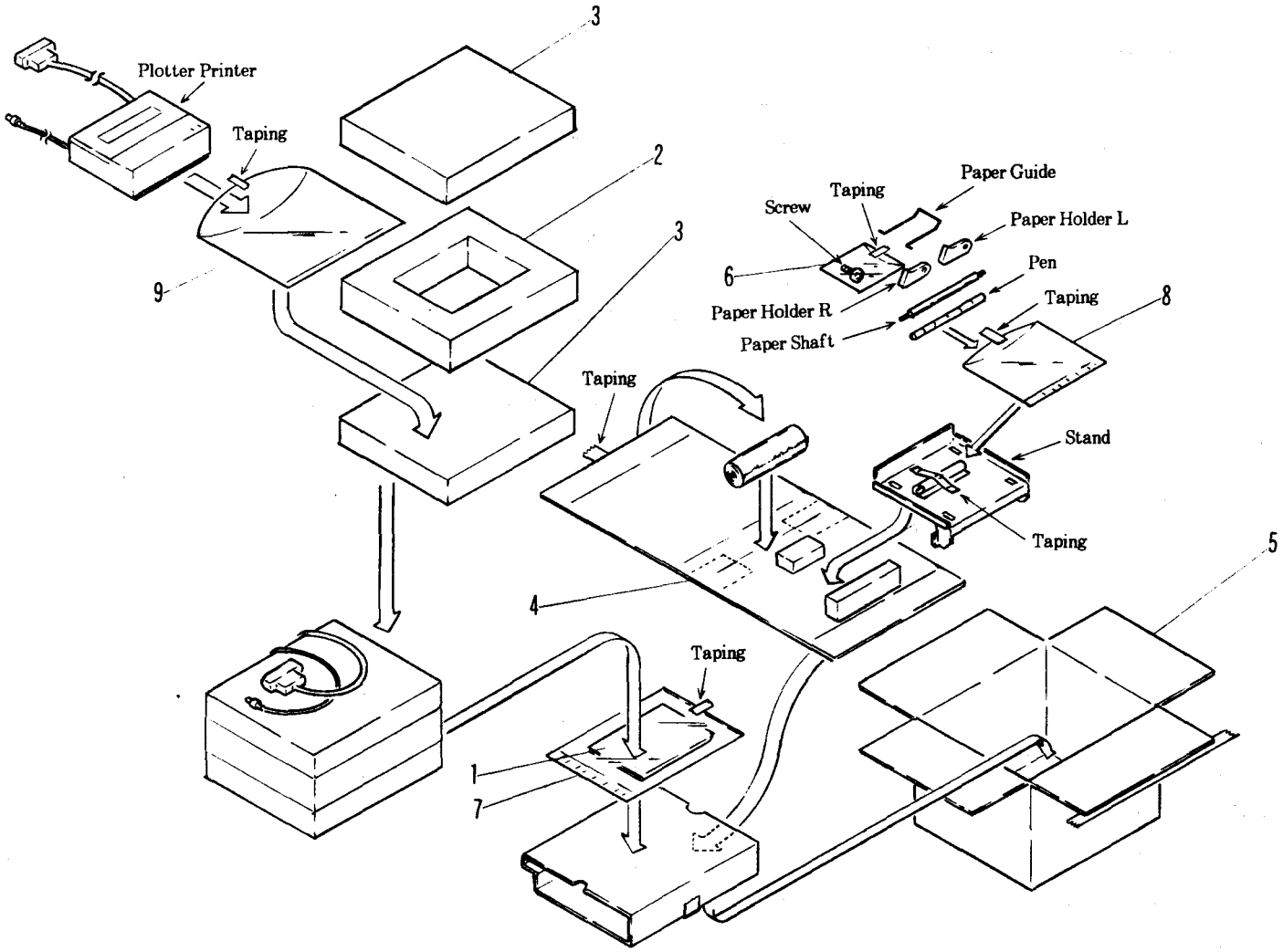
11 MZ-1P16 Main PWB Unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM1009ACZD	AB		C	Connector (4pin)
2	QCNCM1015ACZZ	AC		B	Connector (2pin)
3	QCNCM2414RC2F	AH		C	Connector (26pin)
4	QCNW-1012ACZZ	AL		C	Connector wire
5	QSOCZ6440ACZZ	AG		C	IC socket (40pin)
6	RCRSZ1006ACZZ	AD		C	X-TAL 6MHZ
7	RMPTC8332QCKB	AD		B	Block resistor (3.3KΩ×8 1/8W ±10%)
8	VCCCPU1HH100D	AA		C	Capacitor (50WV 10pF)
9	VCEAAU1AW107Q	AB		C	Capacitor (10V 100μF 6.5φ×10)
10	VCEAAU1HW225Q	AB		C	Capacitor (50WV 2.2μF)
11	VCKYPU1HB331K	AA		C	Capacitor (50WV 330pF)
12	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
13	VHDDS1588L2-1	AB		B	Diode (DS1588L2)
14	VHEHZ11A///-1	AC		B	Zener diode (HZ11A)
15	VHiLB1257///-1	AM		B	IC
16	VHiM5M80500H01	AZ		B	LSI
17	VHiM74LS244-1	AM		B	IC (M74LS244P)
18	VHiSN75451B-1	AG		B	IC (SN75451B)
19	VRD-ST2EY103J	AA		C	Resistor (1/4W 10KΩ ±5%)
20	VRD-ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
21	VRD-ST2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)
22	VRD-ST2EY332J	AA		C	Resistor (1/4W 3.3KΩ ±5%)
23	VRD-ST2EY561J	AA		C	Carbon resistor (1/4W 560Ω ±5%)
24	VRD-ST2EY562J	AA		C	Resistor (1/4W 5.6KΩ ±5%)
25	VS2SA673-C/-1	AE		B	Transistor (2SA673-C)
26	VS2SB739-///-1	AD		B	Transistor
27	VS2SC458KS/-1	AC		B	Transistor (2SC458KS)
28	VS2SD788-C/EC	AC		B	Transistor (2SD788-C/EC)

12 MZ-1P16 Packing Parts

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	TiNSE1213ACZZ	AG	N	D	Instruction book
2	PCUSS1014ACZZ	AL	N	D	Packing cushion A
3	PCUSS1015ACZZ	AH	N	D	Packing cushion B
4	SPAKA1559ACZZ	AH	N	D	Packing accessories
5	SPAKC1560ACZZ	AH	N	D	Packing case
6	SSAKA0006UCZZ	AA		D	Poly bag (50×60mm)
7	SSAKH0015HCZZ	AA		D	Poly bag (180×280mm)
8	SSAKA0231QCZZ	AA		D	Poly bag (80×220 30U)
9	SSAKA2010KCZZ	AA		D	Poly bag (240×300mm)
10	SSAKA5004CCZZ	AA		D	Poly bag (100×300mm)
11	TLABS0918FCZZ	AA		D	F mark label
12	TLABZ1027ACZA	AB	N	D	Pen label
13	TLABJ1083CCZZ	AA		C	Label (U.K. only) (Made in Japan)

12 MZ-1P16 Packing Parts



13 MZ-1E20

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGT1080ACZZ	AK	N	C	PWB angle
2	SPAKA1589ACZZ	AE	N	D	Packing cushion
3	SPAKC1590ACZZ	AT	N	D	Packing case
4	SSAKH3010CCZZ	AA		D	Poly bag (180×240mm)
5	TSELF1002ACZZ	AA		D	Label
6	XBPSD30P06KS0	AA		C	Screw (3×6KS)

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
【C】				
CCABB1006ACZA	10- 1	AM	N	D
CCABB1018ACZB	2- 1	AS		D
CCOVH1002ACZB	1- 1	AQ		D
CFTAT1001ACZA	10- 4	AK	N	D
CSFTZ1001ACZZ	10- 7	AH		E
【D】				
DSOCN0344PAZZ	5- 13	AF		C
DUNT−1409ACZZ	1- 6	BS		B
DUNT−1420ACZZ	1- 7	BM	N	E
DUNT−1421ACZZ	1- 8	BM	N	E
DUNT−1435ACZZ	1- 9	BK		E
DUNTG1412ACZZ	1- 2	AX		D
DUNTG1413ACZZ	1- 3	AX		D
DUNTK1418ACZZ	1- 4	**	N	C
DUNTK1419ACZZ	1- 5	BA	N	C
DUNTK1425ACZZ	10- 16	BF	N	E
DUNTK1426ACZZ	10- 17	AL	N	E
DUNTM1051ACZZ	10- 8	BW		E
【G】				
GCABB1008ACZB	10- 2	AC		C
GCABB1008ACZC	10- 3	AL	N	D
GCOVH1002ACZZ	1- 10	AB		D
GCOVH1009ACZB	1- 34	AN		D
GFTAR1019ACZZ	1- 11	AB		D
GFTAR1021ACZB	1- 35	AE		D
GFTAR1024ACZA	2- 2	AF		D
GFTAR1025ACZZ	1- 12	AC		D
GFTAT1009ACZA	10- 5	AE	N	D
GLEGG1020CCZZ	1- 25	AD		D
GLEGP1001CCZZ	10- 18	AB		C
【H】				
HBDGB1003ACZZ	1- 24	AC		D
HPNLC1004ACZB	1- 36	AE		D
【J】				
JKNBZ1005AC02	10- 9	AG	N	D
【L】				
LANGK1082ACZZ	10- 20	AH	N	C
LANGT1077ACZZ	1- 27	AC		C
LANGT1078ACZZ	1- 28	AC		C
LANGT1079ACZZ	10- 19	AB	N	C
LANGT1080ACZZ	13- 1	AK	N	C
LBNDC0008PAZZ	5- 4	AA		C
LBSHZ2029SCZZ	3- 1	AB		C
LCHSM1010ACZZ	2- 3	AQ		C
LCHSM1016ACZZ	10- 21	AM	N	C
LCHSM1017ACZZ	10- 22	AQ	N	D
LCHSM1018ACZZ	1- 13	AY		C
LHLDZ1002ACL2	10- 10	AB	N	D
LHLDZ1002ACR2	10- 11	AB	N	D
LHLDZ1005ACZZ	2- 4	AD		C
LX−BZ0038FCZZ	10- 37	AA		C
【N】				
NSFTZ1001ACZA	10- 25	AC		C
NSFTZ1001ACZB	10- 26	AG		C
【P】				
PCOVS0181VAZZ	5- 1	AG		C
PCOVS0215PAZZ	5- 2	AF		C
PCUSS1002ACZZ	1- 14	AA		C
PCUSS1014ACZZ	12- 2	AL	N	D
PCUSS1015ACZZ	12- 3	AH	N	D
PCUT−1001ACZA	10- 6	AD	N	D
PGIDW1001ACZZ	10- 12	AB		D
PGUMS1266CCZZ	1- 26	AA		C
PRDAR0143PAZZ	5- 46	AF		C
PRDAR0144PAZZ	5- 47	AE		C
PSPAB1003ACZZ	10- 13	AA		C
PZETE1005ACZZ	10- 14	AA		C
PZETI0021PAZZ	5- 3	AE		C
PZETV1010ACZZ	10- 38	AC	N	C
【Q】				
QACCE3620QCZZ	6- 2	AL		D
QACCZ3321QCN1	6- 1	AL		C
QCNCM1009ACZB	3- 2	AA		C
QCNCM1009ACZD	11- 1	AB		C
QCNCM1009ACZI	3- 3	AC		C
QCNCM1009ACZL	3- 4	AC		C
QCNCM1009ACZO	3- 5	AC		C
QCNCM1010ACZZ	3- 6	AF		C
QCNCM1015ACZZ	11- 2	AC		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QCNCM1038ACZZ	3- 8	AM		C
QCNCM1056ACZZ	1- 29	AG		C
QCNCM2414RC2F	11- 3	AH		C
QCNCW1008AC03	1- 15	AC		C
QCNCW1013ACZZ	3- 7	AC		C
QCNCW1270CC2J	3- 9	AE		C
QCNW−1012ACZZ	11- 4	AL		C
QCNW−1013ACZZ	10- 15	AD		C
QCNW−1049ACZZ	6- 4	AN		C
QCNW−1065ACZZ	6- 3	BA		D
QCNW−1076ACZZ	2- 5	BA		C
QCNW−1108ACZZ	10- 23	AL	N	C
QCNW−1109ACZZ	10- 24	BD	N	C
QCNW−1110ACZZ	10- 34	AE	N	C
QCNW−1111ACZZ	1- 30	AK		C
QCNW−1112ACZZ	1- 31	AG		C
QFS−C0002PAZZ	5- 11	AD		A
QFSHA0001PAZZ	5- 12	AA		C
QJAKC0004PAZZ	5- 14	AD		C
QJAKC1013CCZZ	3- 10	AC		B
QSOCA0003PAZZ	5- 54	AF		C
QSOCZ6418ACZZ	3- 11	AD		C
QSOCZ6428ACZZ	3- 12	AE		C
QSOCZ6440ACZZ	3- 13	AG		C
〃	11- 5	AG		C
QSW−C0003PAZZ	5- 53	AK		B
QSW−K1031ACZZ	1- 16	BH		C
QSW−P1009ACZZ	3- 14	AF		B
QSW−P1010ACZZ	10- 35	AC		C
QSW−P1011ACZZ	10- 36	AD		C
QSW−Z1032ACZZ	1- 32	AM	N	B
QTANS1002ACZZ	1- 17	AD		C
QTANS1003ACZZ	1- 18	AD		C
【R】				
RC−FZ030CPAZZ	5- 25	AE		C
RC−QZ0023PAZZ	5- 28	AD		C
RCRS−1007ACZZ	3- 15	AV		B
RCRSZ1006ACZZ	11- 6	AD		C
RH−iX0464PAZZ	5- 21	AF		B
RH−PX0075PAZZ	5- 52	AK		B
RMPTCB102QCKB	3- 16	AD		B
RMPTC8103QCKB	3- 17	AD		B
RMPTC8332QCKB	11- 7	AD		B
RR−XZ0008PAZZ	5- 29	AB		C
RTPEK1006AC84	6- 18	BB		D
RTRNZ0035PAZZ	5- 16	AE	N	B
RTRNZ0081PAZZ	5- 18	AH		C
RTRNZ0110PAZZ	5- 17	AT		B
RVR−B1450QCZZ	3- 18	AE		B
RVR−M0089PAZZ	5- 19	AC		B
【S】				
SPAKA1559ACZZ	12- 4	AH	N	D
SPAKA1589ACZZ	13- 2	AE	N	D
SPAKA1624ACZL	6- 13	AH	N	D
SPAKA1624ACZR	6- 14	AH	N	D
SPAKA1625ACZZ	6- 15	AM	N	D
SPAKC1552ACZZ	6- 12	AQ	N	D
SPAKC1556ACZZ	6- 11	AQ	N	D
SPAKC1560ACZZ	12- 5	AH	N	D
SPAKC1590ACZZ	13- 3	AT	N	D
SSAKA0006UCZZ	12- 6	AA		D
SSAKA0231QCZZ	6- 17	AA		D
〃	12- 8	AA		D
SSAKA2010KCZZ	12- 9	AA		D
SSAKA5004CCZZ	6- 9	AA		D
〃	12- 10	AA		D
SSAKH0013HCZZ	6- 10	AA		D
SSAKH0014HCZZ	6- 16	AB		D
SSAKH0015HCZZ	12- 7	AA		D
SSAKH3010CCZZ	13- 4	AA		D
【T】				
TINSE1213ACZZ	12- 1	AG	N	D
TINSG1212ACZZ	6- 6	BE	N	D
TINSM1294ACZZ	6- 5	AC	N	D
TLABE1119ACZZ	6- 20	AC		D
TLABE1120ACZZ	6- 21	AC		D
TLABJ1083CCZZ	12- 13	AA		C
TLABS0918FCZZ	12- 11	AA		D
TLABS1128ACZZ	6- 22	AB		D
TLABZ1009ACZC	6- 21	AA		D

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
TLABZ1010ACZZ	6- 7	AD		D	
TLABZ1027ACZA	12- 12	AB	N	D	
TLABZ1102ACZZ	6- 8	AD		D	
TLABZ1103ACZZ	6- 19	AA		D	
TSELF1002ACZZ	13- 5	AA		D	
【V】					
VCCCPU1HH100D	11- 8	AA		C	
VCCCPU1HH101J	3- 35	AB		C	
VCEAAA1AW227M	3- 20	AC		C	
VCEAAA1CW226Q	3- 37	AB		C	
VCEAAU1AM228M	5- 30	AC		C	
VCEAAU1AW107Q	3- 19	AB		C	
〃	11- 9	AB		C	
VCEAAU1CW106Q	3- 36	AB		C	
VCEAAU1EW475Q	3- 21	AB		C	
VCEAAU1HW105Q	3- 38	AB		C	
VCEAAU1HW225Q	11- 10	AB		C	
VCEAAU2GM105M	5- 31	AD		C	
VCEAAU2GM476Y	5- 32	AH		C	
VCKYPU1HB102K	3- 39	AA		C	
VCKYPU1HB331K	11- 11	AA		C	
VCKYPU1HB682K	5- 33	AA		C	
VCKYPU1NB204Z	5- 34	AB		C	
VCKYPU3DB101K	5- 35	AB		C	
VCQYKU1HM102K	5- 36	AA		C	
VCQYKU1HM333K	5- 37	AB		C	
VCSATA1CE226M	3- 40	AB		C	
VCSATA1CE336M	3- 41	AB		C	
VCTYPG1CD104Z	5- 38	AE		C	
VCTYPU1EX103M	3- 42	AB		C	
VCTYPU1EX223M	3- 22	AB		C	
VCTYPU1EX333M	3- 23	AB		C	
VCTYPU1EX473M	3- 24	AB		C	
VCTYPU1NX104M	3- 43	AB		C	
〃	11- 12	AB		C	
VHDDFC05R//-1	5- 39	AC	N	B	
VHDDS1588L1-1	3- 44	AD		B	
VHDDS1588L2-1	9- 4	AB		B	
〃	11- 13	AB		B	
VHDESAC8204-2	5- 48	AN		B	
VHDRB156///-1	5- 20	AG		B	
VHD1S2076A/-1	5- 40	AB		B	
VHEHZ11A///-1	11- 14	AC		B	
VHiCD4069B/-1	3- 45	AE		B	
VHiD65040-032	3- 25	BT		B	
VHiLB1257//-1	11- 15	AM		B	
VHiLH0080A/-1	3- 26	AX		B	
VHiLH0081A/-1	3- 27	AW		B	
VHiLM386N//-1	3- 28	AH		B	
VHiMB81416-12	3- 29	AZ		B	
VHiM5M8050H01	11- 16	AZ		B	
VHiM74LS00/-1	3- 46	AE		B	
VHiM74LS02/-1	3- 47	AE		B	
VHiM74LS04/-1	3- 48	AE		B	
VHiM74LS08/-1	3- 49	AE		B	
VHiM74LS125-1	3- 50	AH		B	
VHiM74LS14/-1	3- 51	AM		B	
VHiM74LS145-1	3- 52	AH		B	
VHiM74LS244-1	11- 17	AM		B	
VHiM74LS245-1	3- 53	AM		B	
VHiM74LS257-1	3- 54	AQ		B	
VHiM74LS32/-1	3- 55	AF		B	
VHiM74LS365-1	3- 56	AF		B	
VHiM74LS74/-1	3- 57	AG		B	
VHiM74LS86/-1	3- 58	AF		B	
VHiNE556N//-1	3- 30	AH		B	
VHiSN74LS373N	3- 59	AL		B	
VHiSN7417N/-1	3- 60	AG		B	
VHiSN75451B-1	11- 18	AG		B	
VHiSN76489/-1	3- 61	AW		B	
VHiUPC358C/-1	9- 38	AG		B	
VHiUPD8255/-1	3- 31	AV		B	
VHi27128/AC85	3- 32	BP		B	
VHi4164-150-H	3- 62	AZ		B	
VHi8253////-1	3- 33	BA		B	
VRD-RU2EE101J	5- 50	AA		C	
VRD-RU2EE151J	5- 26	AA		C	
VRD-RU2EE152J	5- 22	AA		C	
VRD-RV2EY152J	3- 70	AA		C	
VRD-SC2EF151J	5- 24	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VRD-SC2EF180J	5- 23	AA		C	
VRD-SC2EF272J	5- 27	AA		C	
VRD-SC2EF332J	5- 51	AA		C	
VRD-ST2EY000J	3- 63	AA		C	
VRD-ST2EY100J	3- 64	AA		C	
VRD-ST2EY101J	3- 65	AA		C	
VRD-ST2EY102J	3- 66	AA		C	
VRD-ST2EY103J	3- 67	AA		C	
〃	11- 19	AA		C	
VRD-ST2EY104J	3- 68	AA		C	
〃	11- 20	AA		C	
VRD-ST2EY122J	3- 69	AA		C	
VRD-ST2EY182J	3- 71	AA		C	
VRD-ST2EY183J	3- 72	AA		C	
VRD-ST2EY221J	3- 73	AA		C	
〃	11- 21	AA		C	
VRD-ST2EY330J	3- 74	AA		C	
VRD-ST2EY331J	3- 75	AA		C	
VRD-ST2EY332J	3- 76	AA		C	
〃	11- 22	AA		C	
VRD-ST2EY472J	3- 77	AA		C	
VRD-ST2EY473J	3- 78	AA		C	
VRD-ST2EY561J	3- 79	AA		C	
〃	11- 23	AA		C	
VRD-ST2EY562J	11- 24	AA		C	
VRD-ST2EY683J	3- 80	AA		C	
VRD-ST3AF224J	5- 41	AA		C	
VRS-PT3AB1R0J	5- 42	AA		C	
VRS-PT3DB683J	5- 43	AA		C	
VRW-KT3DC100K	5- 44	AC		C	
VSP0080P-608N	1- 19	AN		B	
VS2SA673-C/-1	11- 25	AE		B	
VS2SB739-//-1	11- 26	AD		B	
VS2SC1213-D1A	5- 45	AC		C	
VS2SC3150//-1	5- 49	AK		C	
VS2SC458K//-1	3- 34	AC		B	
VS2SC458KS/-1	11- 27	AC		B	
VS2SD788-C/EC	11- 28	AC		B	
【X】					
XBBSC30P06000	1- 37	AA		C	
〃	2- 6	AA		C	
〃	5- 6	AA		C	
〃	10- 28	AA		C	
XBBSC30P10000	1- 20	AA		C	
XBBSM20P06000	5- 5	AA		C	
XBPSC30P06KS0	5- 10	AA		C	
XBPSC30P06K00	5- 7	AA		C	
XBPSD30P04K00	10- 29	AA		C	
XBPSD30P06KS0	13- 6	AA		C	
XBPSD30P08000	5- 8	AA		C	
XBPSD30P10KS0	2- 7	AB		C	
XBPSD40P08KS0	5- 9	AA		C	
XBPSM30P06KS0	1- 21	AA		C	
〃	1- 33	AA		C	
〃	10- 32	AA		C	
XBPSM30P08K00	1- 22	AA		C	
〃	10- 33	AA		C	
XNESD30-24000	5- 15	AA		C	
XRESJ40-06000	10- 27	AA		C	
XUBSD26P08000	10- 30	AA		C	
XUBSD26P10000	10- 31	AA		C	
XUPSD30P08000	2- 8	AA		C	
XUPSD30P10000	1- 23	AA		C	
【0】					
0BV0210680007	8- 1	AN	N	B	
0BV0211280006	8- 2	AH	N	B	
0BV0222830001	8- 3	AW	N	B	
0BV0364180002	9- 1	AH		B	
0BV0365800008	9- 2	AF	N	B	
0BV0440800004	8- 4	AM	N	B	
0BV0560690004	8- 5	AD	N	B	
0BV0560800009	8- 6	AD	N	B	
0BV0560950005	8- 7	AD		B	
0BV0630121009	8- 8	AA	N	C	
0BV0630220009	8- 9	AA		C	
0BV0630600007	8- 10	AA		C	
0BV0631960001	8- 11	AA		C	
0BV0631982009	8- 12	AA	N	C	
0BV0631992002	8- 13	AA	N	C	
0BV0632060005	8- 14	AA	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
0BV0632070008	8- 15	AA	N	C	
0BV0635110000	8- 16	AA		C	
0BV0636973002	8- 17	AA		C	
0BV0646310006	7- 12	AA	N	C	
0BV0653380009	8- 19	AA		C	
0BV0757170043	7- 1	AA	N	D	
0BV3801290009	8- 20	AC		C	
0BV3801311007	8- 21	AD		C	
0BV3801321000	8- 22	AC		C	
0BV3801331003	8- 23	AC	N	C	
0BV3801341006	8- 24	AD	N	C	
0BV5001700005	8- 25	AA		C	
0BV5624150003	8- 18	AF		C	
0BV6221800005	8- 26	AC	N	C	
0BV6501180009	8- 27	AB		C	
0BV6501361006	8- 28	AD	N	C	
0BV6501372000	8- 29	AC	N	C	
0BV6501380001	8- 30	AB		C	
0BV6501390004	8- 31	AB		C	
0BV6501401009	8- 32	AB	N	C	
0BV6501413004	8- 33	AB	N	C	
0BV6501461007	8- 36	AG		C	
0BV6501471000	8- 34	AE		C	
0BV6501480002	8- 35	AF		C	
0BV6501832003	8- 37	AC		C	
0BV6501841005	8- 38	AC	N	C	
0BV6502030006	8- 39	AB		C	
0BV6502251005	8- 40	AD	N	C	
0BV6502300505	8- 41	AK	N	C	
0BV6502584000	8- 42	AF	N	C	
0BV6502595004	8- 43	AF	N	C	
0BV6502620009	8- 44	AB		C	
0BV6502660001	8- 45	AB		C	
0BV6502752001	8- 46	AG	N	C	
0BV6502920002	8- 47	AF	N	C	
0BV6502930005	8- 48	AF	N	C	
0BV6502940008	8- 49	AA	N	C	
0BV6611820002	7- 2	AC	N	C	
0BV6628620024	8- 50	AD	N	C	
0BV6661050008	8- 51	AG	N	C	
0BV6661410000	8- 52	AB	N	C	
0BV6674000003	8- 53	AA	N	C	
0BV6680010005	7- 10	BG	N	E	
0BV6680400017	7- 11	BP	N	E	
0BV6681000005	8- 54	AS	N	C	
0BV6681200007	8- 55	AE	N	C	
0BV6682700005	8- 56	AG	N	C	
0BV6685400001	7- 13	AG	N	C	
0BV6688000017	7- 3	AT	N	D	
0BV6688040019	7- 4	AL	N	D	
0BV6688220015	7- 5	AC	N	D	
0BV9020045558	9- 39	AD	N	B	
0BV9020046250	9- 3	AF	N	B	
0BV9110340008	9- 5	AK	N	B	
0BV9205118149	9- 6	AA	N	C	
0BV9208610248	9- 7	AA	N	C	
0BV9208610341	9- 8	AA	N	C	
//	9- 8	AA	N	C	
0BV9208615140	9- 9	AA	N	C	
0BV9208615346	9- 10	AA	N	C	
0BV9208615449	9- 11	AA	N	C	
0BV9208620540	9- 12	AA	N	C	
0BV9208622243	9- 13	AA	N	C	
0BV9208622346	9- 14	AA	N	C	
0BV9208622449	9- 15	AA	N	C	
0BV9208627145	9- 16	AA	N	C	
0BV9208633144	9- 17	AA	N	C	
0BV9208647048	9- 18	AA	N	C	
0BV9208647141	9- 19	AA	N	C	
0BV9208647347	9- 20	AA	N	C	
0BV9208656040	9- 21	AA	N	C	
0BV9208656246	9- 22	AA	N	C	
0BV9208656442	9- 23	AA	N	C	
0BV9208682148	9- 24	AA	N	C	
0BV9208682241	9- 25	AA	N	C	
0BV9227120142	9- 26	AC	N	C	
0BV9250347046	9- 27	AB	N	C	
0BV9298020174	9- 28	AD	N	C	
0BV9318310250	9- 29	AC	N	C	
0BV9318347359	9- 30	AC	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
0BV9349010161	9- 31	AD	N	C	
0BV9349022063	9- 32	AC		C	
0BV9349047064	9- 33	AD	N	C	
0BV9349210060	9- 34	AC		C	
0BV9349501061	9- 35	AC		C	
0BV9349510960	9- 36	AC		C	
0BV9710200254	8- 57	AA	N	C	
0BV9710200313	8- 58	AA		C	
0BV9710200416	8- 59	AA		C	
0BV9710200519	8- 60	AA		C	
0BV9710260414	7- 6	AA		C	
0BV9711260417	7- 7	AA		C	
0BV9712200412	8- 61	AA		C	
0BV9718200410	8- 62	AA		C	
0BV9718260511	7- 8	AA	N	C	
0BV9743551004	8- 63	AA		C	
0BV9760260811	8- 64	AA		C	
0BV9760261018	7- 9	AA	N	C	
0BV9799024006	8- 65	AA	N	C	
0BV9811015142	8- 66	AA		C	
0BV9811025145	8- 67	AA		C	
0BV9811030143	8- 68	AA		C	
0BV9862020115	8- 69	AA	N	C	
0BV9870003003	8- 70	AA		C	
0BV9870012005	8- 71	AA	N	C	
0BV9874002004	8- 72	AA		C	
0BV9874026004	8- 73	AA		C	
0BV9905210051	9- 37	AD	N	C	

SHARP

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